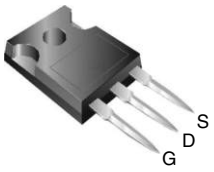
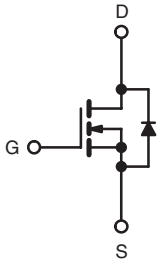
# Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 500 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 10 V | 0.27 |
| $Q_g$ (Max.) (nC) | 105 | |
| $Q_{gs}$ (nC) | 26 | |
| $Q_{gd}$ (nC) | 42 | |
| Configuration | Single | |

TO-247




N-Channel MOSFET

## FEATURES

- Low Gate Charge $Q_g$ Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective $C_{oss}$ Specified
- Compliant to RoHS Directive 2002/95/EC

Available

RoHS* COMPLIANT

## APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High Speed Power Switching

## TYPICAL SMPS TOPOLOGIES

- Full Bridge
- PFC Boost

| ORDERING INFORMATION | |
|---|---|
| Package | TO-247 |
| Lead (Pb)-free | IRFP460APbF |
| | SiHFP460A-E3 |
| SnPb | IRFP460A |
| | SiHFP460A |

**ABSOLUTE MAXIMUM RATINGS** $T_C$ = 25 °C, unless otherwise noted

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DS}$ | 500 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 30 | |
| Continuous Drain Current | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 20 | A |
| | | $T_C$ = 100 °C | | 13 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | 80 | |
| Linear Derating Factor | | | | 2.2 | W/°C |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 960 | mJ |
| Repetitive Avalanche Current[a] | | | $I_{AR}$ | 20 | A |
| Repetitive Avalanche Energy[a] | | | $E_{AR}$ | 28 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 280 | W |
| Peak Diode Recovery dV/dt[c] | | | dV/dt | 3.8 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) | for 10 s | | | 300[d] | |
| Mounting Torque | 6-32 or M3 screw | | | 10 | lbf · in |
| | | | | 1.1 | N · m |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Starting $T_J$ = 25 °C, L = 4.3 mH, $R_g$ = 25 Ω, $I_{AS}$ = 20 A (see fig. 12).

c. $I_{SD} \leq$ 20 A, dI/dt ≤ 125 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.

d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 40 | °C/W |
| Case-to-Sink, Flat, Greased Surface | $R_{thCS}$ | 0.24 | - | |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 0.45 | |

| **SPECIFICATIONS** $T_J$ = 25 °C, unless otherwise noted | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | | 500 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | | - | 0.61 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 30 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 500 V, $V_{GS}$ = 0 V | | - | - | 25 | µA |
| | | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 12 A[b] | - | - | 0.27 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 12 A[b] | | 11 | - | - | S |
| **Dynamic** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | | - | 3100 | - | pF |
| Output Capacitance | $C_{oss}$ | | | - | 480 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | - | 18 | - | |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | $V_{DS}$ = 1.0 V, f = 1.0 MHz | | 4430 | | |
| | | | $V_{DS}$ = 400 V, f = 1.0 MHz | | 130 | | |
| Effective Output Capacitance | $C_{oss}$ eff. | | $V_{DS}$ = 0 V to 400 V[c] | | 140 | | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V | $I_D$ = 20 A, $V_{DS}$ = 400 V, see fig. 6 and 13[b] | - | - | 105 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | - | - | 26 | |
| Gate-Drain Charge | $Q_{gd}$ | | | - | - | 42 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 250 V, $I_D$ = 20 A, $R_G$ = 4.3 Ω, $R_D$ = 13 Ω, see fig. 10[b] | | - | 18 | - | ns |
| Rise Time | $t_r$ | | | - | 55 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 45 | - | |
| Fall Time | $t_f$ | | | - | 39 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 20 | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | | - | - | 80 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 20A, $V_{GS}$ = 0 V[b] | | - | - | 1.8 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 20 A, dI/dt = 100 A/µs[b] | | - | 480 | 710 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | | - | 5.0 | 7.5 | µC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

c. $C_{oss}$ eff. is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DS}$.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

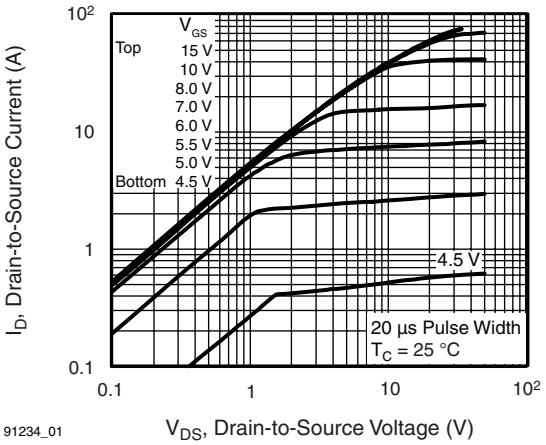



**Fig. 1 - Typical Output Characteristics**

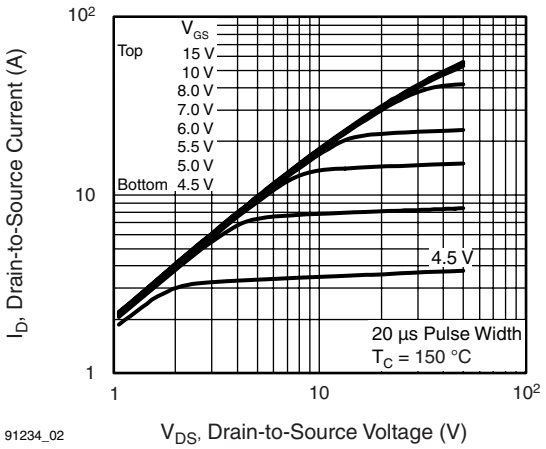



**Fig. 2 - Typical Output Characteristics**

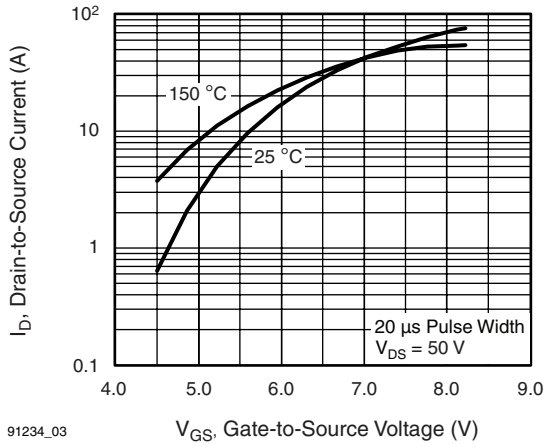



**Fig. 3 - Typical Transfer Characteristics**

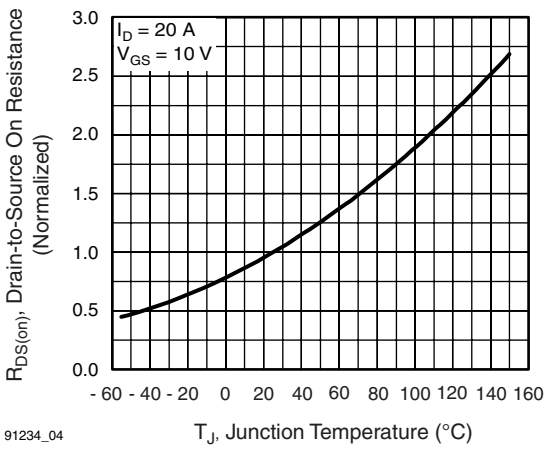



**Fig. 4 - Normalized On-Resistance vs. Temperature**

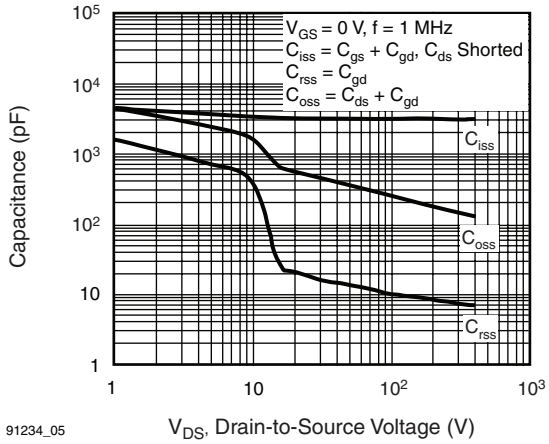



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

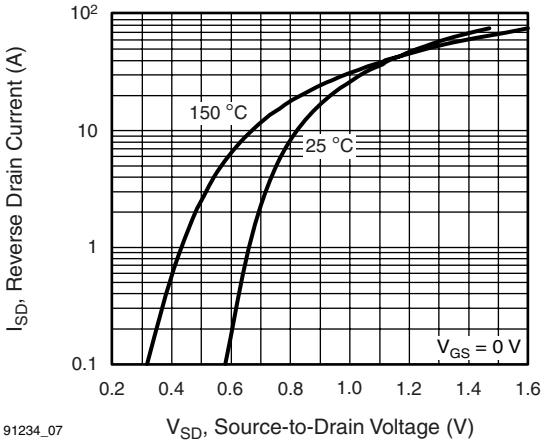



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

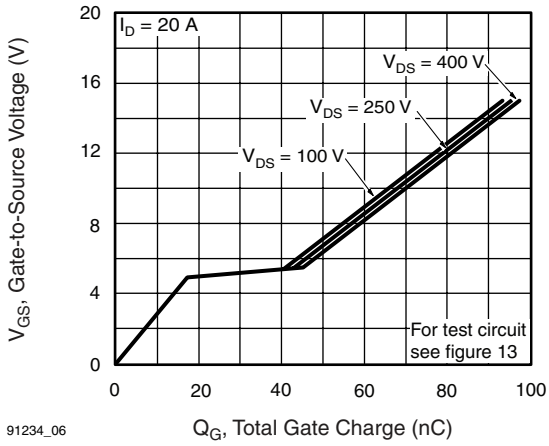



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

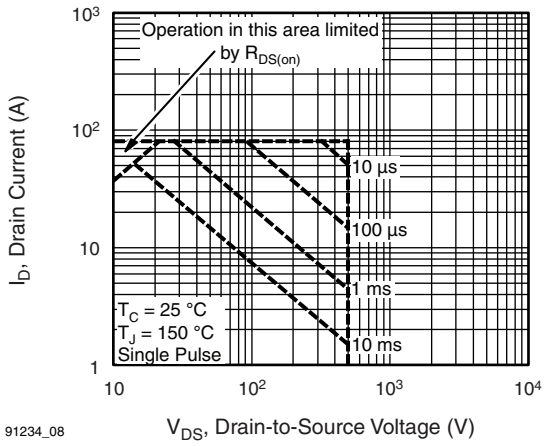



**Fig. 8 - Maximum Safe Operating Area**

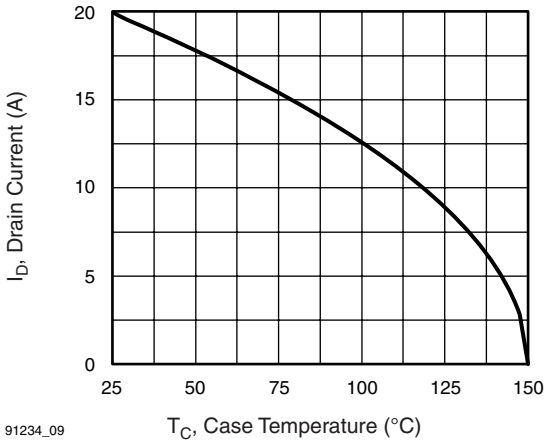



**Fig. 9 - Maximum Drain Current vs. Case Temperature**

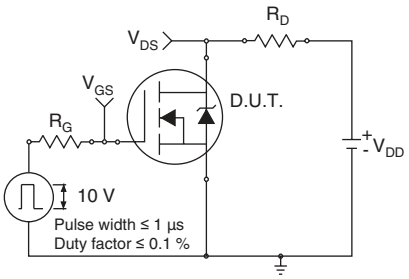



**Fig. 10a - Switching Time Test Circuit**

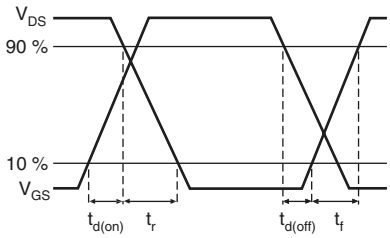



**Fig. 10b - Switching Time Waveforms**

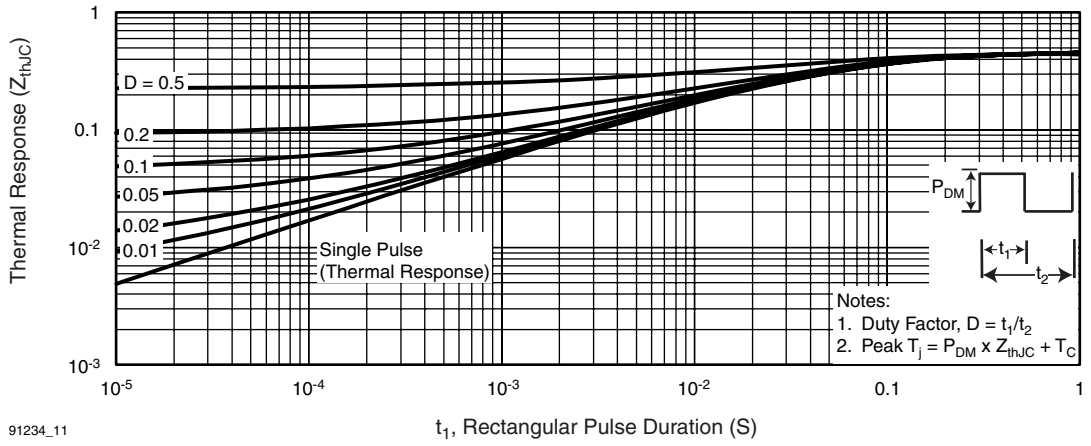



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

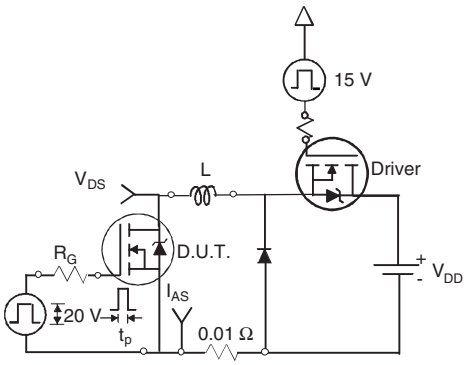



**Fig. 12a - Unclamped Inductive Test Circuit**

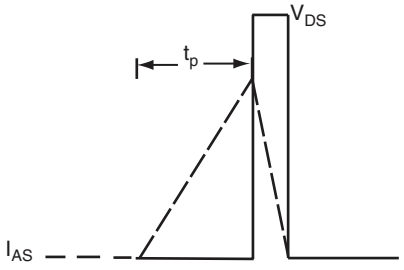



**Fig. 12b - Unclamped Inductive Waveforms**

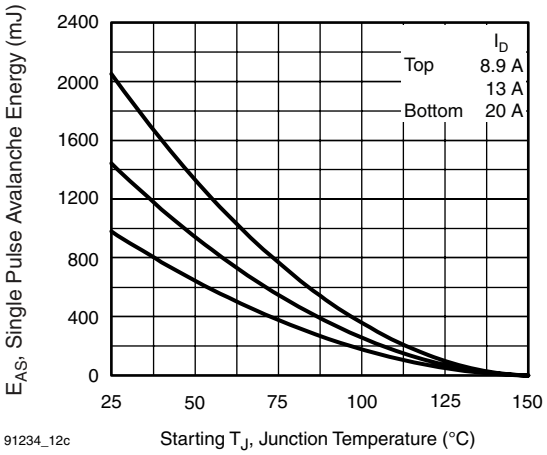



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

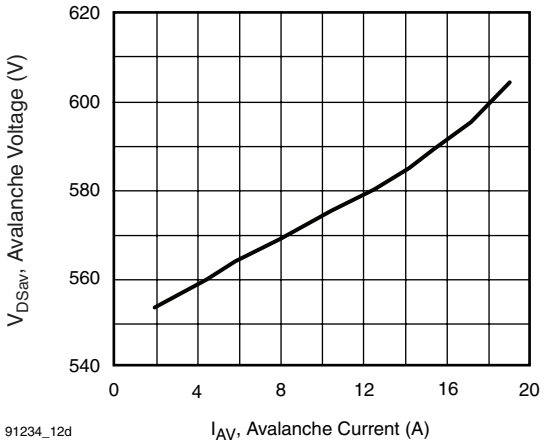



**Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current**

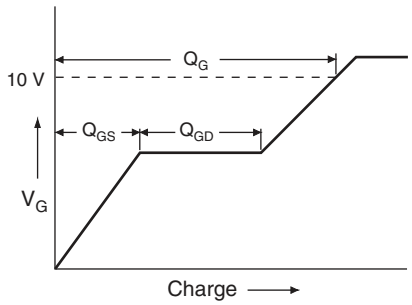



**Fig. 13a - Basic Gate Charge Waveform**

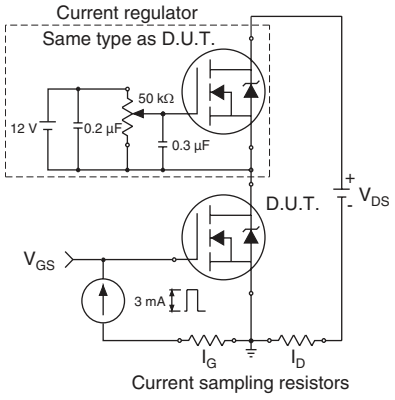
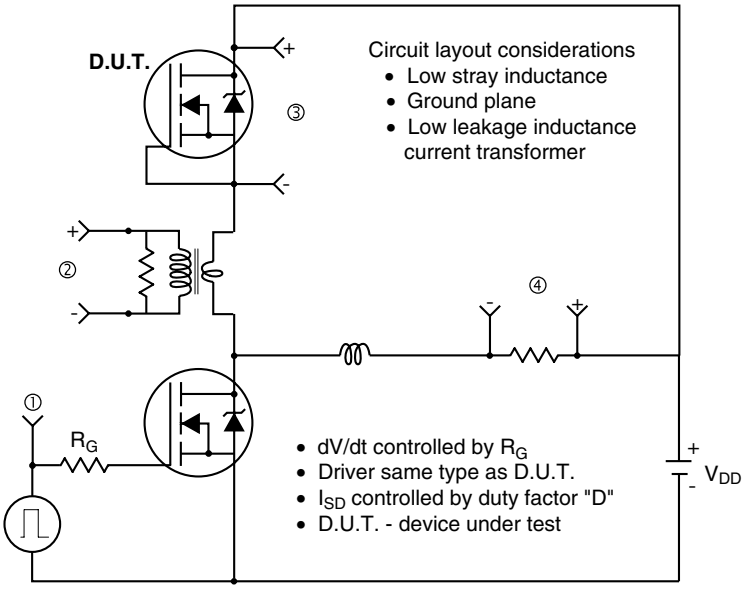
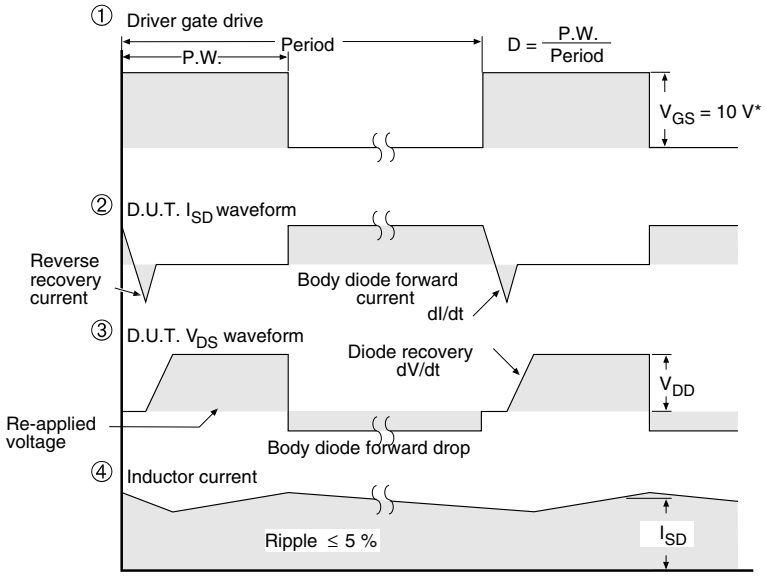



**Fig. 13b - Gate Charge Test Circuit**

## Peak Diode Recovery dV/dt Test Circuit



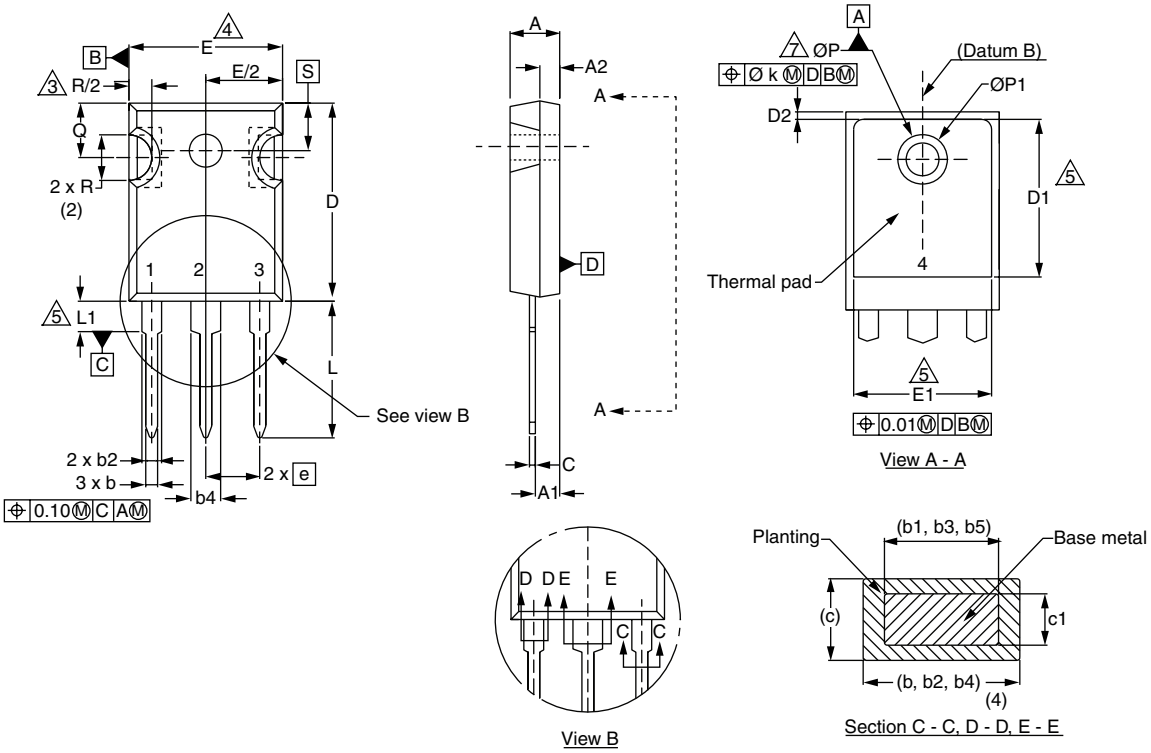




* $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91234.*

## TO-247AC (HIGH VOLTAGE)




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 4.65 | 5.31 | 0.183 | 0.209 |
| A1 | 2.21 | 2.59 | 0.087 | 0.102 |
| A2 | 1.50 | 2.49 | 0.059 | 0.098 |
| b | 0.99 | 1.40 | 0.039 | 0.055 |
| b1 | 0.99 | 1.35 | 0.039 | 0.053 |
| b2 | 1.65 | 2.39 | 0.065 | 0.094 |
| b3 | 1.65 | 2.37 | 0.065 | 0.093 |
| b4 | 2.59 | 3.43 | 0.102 | 0.135 |
| b5 | 2.59 | 3.38 | 0.102 | 0.133 |
| c | 0.38 | 0.86 | 0.015 | 0.034 |
| c1 | 0.38 | 0.76 | 0.015 | 0.030 |
| D | 19.71 | 20.70 | 0.776 | 0.815 |
| D1 | 13.08 | - | 0.515 | - |

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D2 | 0.51 | 1.30 | 0.020 | 0.051 |
| E | 15.29 | 15.87 | 0.602 | 0.625 |
| E1 | 13.72 | - | 0.540 | - |
| e | 5.46 BSC | | 0.215 BSC | |
| Ø k | 0.254 | | 0.010 | |
| L | 14.20 | 16.10 | 0.559 | 0.634 |
| L1 | 3.71 | 4.29 | 0.146 | 0.169 |
| N | 7.62 BSC | | 0.300 BSC | |
| Ø P | 3.56 | 3.66 | 0.140 | 0.144 |
| Ø P1 | - | 7.39 | - | 0.291 |
| Q | 5.31 | 5.69 | 0.209 | 0.224 |
| R | 4.52 | 5.49 | 0.178 | 0.216 |
| S | 5.51 BSC | | 0.217 BSC | |

ECN: S-81920-Rev. A, 15-Sep-08
DWG: 5971

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.

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