AVR504: Migrating from ATtiny26 to ATtiny261/461/861

8-bit AVR® Microcontrollers

Application Note

Features

- General Porting Considerations
- Memories
- System Clock and Clock Options
- System Control and Reset
- Registers
- Interrupts
- Timer/Counters
- USI – Universal Serial Interface
- Analogue-to-Digital Converter
- I/O Ports
- Memory Programming
- Electrical Characteristics

1 Introduction

This application note is a guide to assist users of ATtiny26 in converting existing designs to ATtiny261. The document will also assist ATtiny26 users to migrate to the ATtiny461 and ATtiny861 devices, which are members of the same family as the ATtiny261, offering larger memories.

In addition to the differences described in this document, the electrical characteristics of the devices are different. Some of these differences are outlined in this document and some are not. Please check the latest data sheets for detailed information.

Improvements or added features in ATtiny261 that are not in conflict with those in ATtiny26 are not listed in this document.

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2 General Porting Considerations

Between the devices described in this application note, some registers and register bits have changed name but note that they preserve the same functionality. They are all listed later in this document.

To make the porting process as easy as possible, always refer to registers and bit positions using their defined names. Avoid using absolute addresses and values. In most cases, the register and bit names are unchanged from device to device. When you are porting a design, it is more convenient to include the correct definition file for the new device, rather than manually changing all your addresses and bit values. It is also considered good programming practice to use named references instead of absolute values. Some examples are shown below.

```
PORTB |=  (1<<PORTB3);          // Set pin 3 on port B high
DDRB  &= ~(1<<PORTB3);          // Set pin 3 on port B as input


// Configure USI
USICR  =  (1<<USISIE)|(0<<USIOIE)|(1<<USIWM1)|(0<<USIWM0)|
          (1<<USICS1)|(0<<USICS0)|(0<<USICLK)|(0<<USITC);
```

To avoid conflicts with added features and register functionality, never access registers that are marked as reserved. Reserved bits should always be written to zero if accessed. This ensures forward compatibility, and added features will stay in their default states when unused.

3 Memories

ATtiny26 and ATtiny261 have the same amount of volatile and non-volatile memory. ATtiny461 and ATtiny861 have more SRAM, Flash and EEPROM than ATtiny26. Applications that rely on the size of memory may therefore misbehave when memory size is increased. For example, this may be the case with wrap-around indexing of EEPROM.

3.1 Stack

The ATtiny26 stack pointer is implemented as an 8-bit register in the I/O space. In ATtiny261 the stack pointer is also realised as one 8-bit register, but in ATtiny461 and ATtiny861 the amount of data memory exceeds the 8-bit address range and the stack pointer has been realised as two 8-bit registers. See table below.

Table 3-1. Device Stack Pointers.

<table>
<tr><th>Device</th><th>Low Stack Pointer</th><th>High Stack Pointer</th></tr>
<tr><td>ATtiny26</td><td>SP</td><td rowspan="2">N/a</td></tr>
<tr><td>ATtiny261</td><td rowspan="3">SPL</td></tr>
<tr><td>ATtiny461</td><td rowspan="2">SPH</td></tr>
<tr><td>ATtiny861</td></tr>
</table>

See ATtiny261/461/861 data sheet for information on how to access stack pointer registers.

3.2 EEPROM

EEPROM write access times depend on the frequency of the internal RC oscillator. In ATtiny261/461/861 the access times are shorter than in ATtiny26.

ATtiny261 is part of a pin and functionally compatible subfamily of tinyAVR®, where the size of EEPROM ranges from 128 to 512 bytes. This means more than eight data bits are required for memory addressing and, therefore, the EEPROM address register has been expanded from one 8-bit register (EEAR in ATtiny26) to two (EEARL and EEARH in ATtiny261, ATtiny461 and ATtiny861). Since the initial values of the registers are undefined it is important to always write both registers even when accessing only the bottom section of the EEPROM.

4 System Clock and Clock Options

ATtiny261/461/861 has a more advanced clock system than ATtiny26. In ATtiny261/461/861 there is a system clock prescaler and two internal clock sources.

4.1 Clock Sources

Clock source options are set differently in ATtiny261/461/861. See table below.

Table 4-1. Clock Source Settings.

<table>
<tr><th colspan="3">ATtiny26</th><th colspan="2">ATtiny261/461/861</th></tr>
<tr><th>Clocking Option</th><th>PLLCK</th><th>CKSEL[3:0]</th><th>CKSEL[3:0]</th><th>CLKPS[3…0]</th></tr>
<tr><td>PLL</td><td>0</td><td>0001</td><td>0001</td><td>0000</td></tr>
<tr><td>External Clock</td><td>1</td><td>0000</td><td>0000</td><td>0000</td></tr>
<tr><td>Internal RC Oscillator, 1 MHz</td><td>1</td><td>0001</td><td rowspan="4">0010</td><td>0011</td></tr>
<tr><td>Internal RC Oscillator, 2 MHz</td><td>1</td><td>0010</td><td>0010</td></tr>
<tr><td>Internal RC Oscillator, 4 MHz</td><td>1</td><td>0011</td><td>0001</td></tr>
<tr><td>Internal RC Oscillator, 8 MHz</td><td>1</td><td>0100</td><td>0000</td></tr>
<tr><td>External RC Oscillator, 0.1…0.9 MHz</td><td>1</td><td>0101</td><td rowspan="4" colspan="2">Not available, use internal RC oscillator instead</td></tr>
<tr><td>External RC Oscillator, 0.9…3.0 MHz</td><td>1</td><td>0110</td></tr>
<tr><td>External RC Oscillator, 3.0…8.0 MHz</td><td>1</td><td>0111</td></tr>
<tr><td>External RC Oscillator, 8.0…12.0 MHz</td><td>1</td><td>1000</td></tr>
<tr><td>External Low-Frequency Oscillator, 32.768 kHz</td><td>1</td><td>1001</td><td>01xx</td><td>0000</td></tr>
<tr><td rowspan="2">External Resonator Oscillator, 0.4…0.9 MHz</td><td>1</td><td>1010</td><td rowspan="2">1000
1001</td><td>0000</td></tr>
<tr><td>1</td><td>1011</td><td>0000</td></tr>
<tr><td rowspan="2">External Crystal/Resonator Oscillator, 0.9…3.0 MHz</td><td>1</td><td>1100</td><td rowspan="2">1010
1011</td><td>0000</td></tr>
<tr><td>1</td><td>1101</td><td>0000</td></tr>
<tr><td rowspan="2">External Crystal/Resonator Oscillator, 3.0…16.0 MHz</td><td>1</td><td>1110</td><td rowspan="2">1100, 1101
1110, 1111</td><td>0000</td></tr>
<tr><td>1</td><td>1111</td><td>0000</td></tr>
</table>

4.2 Calibration of Internal RC Oscillator

The frequency of the internal RC oscillator of ATtiny261/461/861 can be calibrated using the OSCCAL register, similarly as in ATtiny26. The only difference is that in ATtiny261/461/861 the highest bit (CAL7) determines the range of operation, while in

ATtiny26 all eight bits of the OSCCAL register are used to adjust the frequency within one, single range.

4.3 High Frequency PLL Clock

When using the internal PLL as a clock source, ATtiny261/461/861 applies a longer start-up delay than ATtiny26 after a power-on reset and power-down wakeup. This is to ensure stable and glitch-free operation.

5 System Control and Reset

ATtiny261/461/861 has more fuse bits than ATtiny26. In addition, some fuse bits have a different functionality.

5.1 Brown-Out Detection (BOD)

Both ATtiny26 and ATtiny261/461/861 have programmable Brown-Out Detection levels. The programming method and levels are not entirely the same. See table below.

Table 5-1. Brown-Out Detection (BOD) Characteristics.

ATtiny26			ATtiny261/461/861	
BODEN	**BODLEVEL**	**V_{BOT}**	**BODLEVEL[2…0]**	**V_{BOT}**
1	X	Disabled	111	Disabled
0	0	4.0 V	100	4.3 V
	1	2.7 V	101	2.7 V

5.2 Start-up Times & Brown-out Detection

Due to electrical differences between ATtiny26 and ATtiny261/461/861 there may be minor dissimilarities in start-up times. Please see device data sheets for more detailed information.

5.3 Power-On Reset

The threshold levels of power-on reset are not identical for ATtiny26 and ATtiny261/461/861. The power-on threshold voltage is slightly lower on ATtiny261/461/861.

Please see device data sheets for more detailed information.

5.4 Watchdog Timer

The ATtiny261/461/861 includes an enhanced Watchdog Timer (WDT), compared to the watchdog timer used in ATtiny26. At 5V operating voltage the WDT will behave similar on ATtiny26 and ATtiny261/461/861. At lower voltages the watchdog timeout interval may differ. Please see data sheet for characteristic data on watchdog oscillator frequency.

If the WDT is not used, it is still recommended to disable it initially in the application code to clear unintentional WDT enabled events.

6 Registers

Some of the register names have changed and some registers have moved.

6.1 Renamed Registers

The below tables list the registers which have been renamed but still exist at the same physical address and have maintained their functionality. It is only required to update the register name in the application.

Table 6-1. Changes to Register Names.

Address [hex]	Name in ATtiny26	Name in ATtiny261/461/861
0x06	ADCSR	ADCSRA
0x08	ACSR	ACSRA
0x1E	EEAR	EEARL
0x1F	-	EEARH
0x32	TCNT0	TCNT0L
0x33	TCCR0	TCCR0B
0x3D	SP	SPL

6.2 Renamed Bits

The below table lists the bits that have been renamed, but still exist in the same register and in the same register location.

Table 6-2. Changes to Bit Names.

ATtiny26			ATtiny261/461/861
Bit Name	**Register**	**Address**	**Bit Name**
ADFR	ADCSR	0x06	ADATE
USISIF	USISR	0x0E	USICIF
EEMWE	EECR	0x1C	EEMPE
EEWE	EECR	0x1C	EEPE

6.3 Removed Bits

The below table lists register bits, which have been removed and have no close replacements.

Table 6-3. ATtiny26 Removed Register Bits and Functions.

Register Name	Register Bit	Function
TCCR1B	CTC1	Resets Timer/Counter1

7 Interrupts

Interrupt handling has been improved in ATtiny261/461/861.

7.1 Interrupt Vectors

ATtiny261/461/861 has more interrupt vectors than ATtiny26, but all ATtiny26 vectors exist in identical locations on ATtiny261/461/861. Programs can still use the end of ATtiny26 interrupt vector table as a starting address on ATtiny261/461/861, provided that ATtiny261/461/861 specific interrupts are not enabled.

7.2 Pin Change Interrupt

Pin change interrupts are automatically disabled on ATtiny26 if an alternative function has been enabled for the given pin. In ATtiny261/461/861 this is not the case, where alternative pin functions and pin change interrupts may be concurrently enabled for the same pin. Pin change interrupts for a given pin in ATtiny261/461/861 are masked and unmasked using Pin Change Mask Register A (PCMSKA) and Pin Change Mask Register B (PCMSKB).

7.2.1 Source Pins and Masking

ATtiny261/461/861 extends pin change interrupts to cover all I/O pins, while ATtiny26 only includes pins PA3, PA6…7 and PB0…7. Also, ATtiny261/461/861 allows individual masking of pin change interrupt sources via registers PCMSK0 and PCMSK1 (a feature not found in ATtiny26) but the default setting is to enable only those sources that are common for both ATtiny26 and ATtiny261/461/861.

8 Timer/Counters

Timer/Counter1 has been improved in ATtiny261/461/861.

8.1 Timer/Counter1

In ATtiny261/461/861 the synchronisation registers are not bypassed as in ATtiny26. This means a synchronisation delay of 1.5 clock cycles is present in both asynchronous and synchronous modes.

8.1.1 Bit CTC1 of Register TCCR1B

Bit CTC1 of register TCCR1B has been replaced by PWM1X on ATtiny261/461/861. Please note that these bits have a different functionality and that this must be considered during migration.

8.1.2 Register OCR1C

Register OCR1C is now always the TOP value for the timer/counter and the register is always reset (cleared to zero) after reaching the TOP value.

The lowest allowed TOP value is 3. If register OCR1C is loaded with a value lower than 3 it will be forced to the value 3. Also note that after a reset the OCR1C register is loaded with the timer/counter MAX value, which means that the default TOP value is 0x3FF.

8.1.3 PWM Mode

When writing to register OCR1C on ATtiny261/461/861 the data is buffered and the register updated only when OCR1C has reached the TOP value. In ATtiny26 writing to OCR1C is immediate.

9 USI – Universal Serial Interface

The ATtiny261/461/861 uses an enhanced version of the Universal Serial Interface, as compared to the ATtiny26.

9.1 Clock Sources

The USI clock can be selected from three different sources, two of which are common for ATtiny26 and ATtiny261/461/861. The third clock source option (USICS[2:0] = 01X) in ATtiny26 is Timer/Counter0 Overflow, but in ATtiny261/461/861 it has been replaced by Timer/Counter0 Compare Match. Similar functionality can be achieved but it may be necessary to update any parts of firmware that refer to Timer/Counter0 overflow flags and interrupts.

10 Analogue-to-Digital Converter

The Analogue-to-Digital Converter (ADC) has been enhanced and in ATtiny261/461/861 includes more features. ATtiny261/461/861 is a 1.8V device and the default internal voltage reference is therefore set to 1.1V.

10.1 Voltage Reference Selection

Voltage reference source is selected using bits REFS2…0, located in registers ADMUX (ADC Multiplexer Selection) and ADCSRB (ADC Control and Status Register B). ATtiny26 only includes bits REFS1…0. The table below shows how to update reference selection bits to maintain functionality.

Table 10-1. Setting Voltage Reference Source.

ATtiny26	**ATtiny261/461/861**	**Voltage Reference**
REFS1…0	**REFS2…0**	
00	000	AVCC
01	001	AREF (internal reference turned off)
10	110	Internal 2.56V reference (AREF disconnected)
11	111	Internal 2.56V reference (AREF connected)

11 I/O Ports

Test limits for port drive strength are lower on ATtiny261/461/861. This means ATtiny261/461/861 ports are rated for a lower current than ATtiny26. Port driver characteristics are outlined in the table below.

Table 11-1. Port Drive Characteristics.

Condition	Pin Rating [mA]		Sum Rating [mA]	
	ATtiny26	ATtiny261/461/861	ATtiny26	ATtiny261/461/861
V_{CC} = 5V	20 mA	10 mA	400 mA	60 mA
V_{CC} = 3V	10 mA	5 mA		

12 Memory Programming

Some modifications regarding the programming of fuse and calibration bytes msut be taken into account. Also, the functionality of the calibration byte has been changed.

12.1 Fuse Bits

The number of fuse bits has been increased and fuse bits are scattered over three bytes in ATtiny261/461/861. Read and write algorithms must be updated for proper fuse programming.

The functionality of the following fuse bits has changed:

- The BODLEVEL fuse bit of ATtiny26 has been expanded to three fuse bits (BODLEVEL2…0) on ATtiny261/461/861.
- The BODEN fuse bit functionality of ATtiny26 has been integrated into BODLEVEL2…0 fuse bits of ATtiny261/461/861.
- The PLLCK and CKOPT fuse bit functionality of ATtiny26 has been integrated into CKSEL3…0 fuse bits of ATtiny261/461/861.
- Clock prescaler functionality of CKSEL fuses has been removed, since ATtiny261/461/861 has a software configurable clock prescaler.

12.2 Signature Bytes

Signature bytes reside in a separate address space and can only be read external to the device. Therefore, this notion only applies to programmers, et al, and not to the actual program being migrated.

Signature bytes have been updated as illustrated in the table below.

Table 12-1. Summary of Signature Bytes.

Byte	ATtiny26	ATtiny261	ATtiny461	ATtiny861
$000	$1E	$1E	$1E	$1E
$001	$91	$91	$92	$93
$002	$09	$0C	$08	$0D

12.3 Calibration Byte

ATtiny26 has four calibration bytes for the 1MHz, 2MHz, 4MHz and 8MHz operation of the internal RC oscillator. ATtiny261/461/861 only has one calibration byte for the internal RC oscillator.

13 Electrical Characteristics

ATtiny261/461/861 is manufactured using a different process than ATtiny26 and electrical characteristics will therefore differ between these devices. Please consult the data sheets for details on electrical characteristics.

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