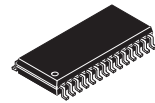




MC9RS08LE4



28 W-SOIC
Case 751F

MC9RS08LE4

Features:

- 8-Bit RS08 Central Processor Unit (CPU)
 - Up to 20 MHz CPU at 2.7 V to 5.5 V across temperature range of -40°C to 85°C
 - Subset of HC08 instruction set with added BGND instructions
- On-Chip Memory
 - 4 KB flash memory read/program/erase over full operating voltage and temperature
 - 256-byte random-access memory (RAM)
 - Security circuitry to prevent unauthorized access to flash memory contents
- Power-Saving Modes
 - Wait and stop
- Clock Source Options
 - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 1 MHz to 20 MHz
 - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies up to 10 MHz
- System Protection
 - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
 - Low-voltage detection with reset or interrupt
 - Selectable trip points
 - Illegal opcode detection with reset
 - Illegal address detection with reset
 - Flash memory block protection
- Development Support
 - Single-wire background debug interface
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
 - **LCD** — Up to 8×14 or 4×18 segments; compatible with 5 V or 3 V LCD glass displays using on-chip resistor bias network; functional in wait, stop modes for very low power LCD operation; frontplane and backplane pins multiplexed with GPIO functions; selectable frontplane and backplane configurations
 - **ADC** — 8-channel, 10-bit resolution; 2.5 μs conversion time; automatic compare function; 1.7 mV/ $^{\circ}\text{C}$ temperature sensor; internal bandgap reference channel; operation in stop; fully functional from 2.7 V to 5.5 V.
 - **TPM** — Two 2-channel 16-bit timer/pulse-width modulator (TPM) modules; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
 - **SCI** — One serial communications interface module with optional 13-bit break; LIN extensions
 - **KBI** — 8-pin keyboard interrupt module
- Input/Output
 - 26 GPIOs including 1 output-only pin and 1 input-only pin
 - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package Options
 - 28-pin SOIC

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

| Revision | Date | Description of Changes |
|----------|-----------|---|
| 1 | 10/6/2008 | Initial public release. |
| 2 | 11/3/2008 | In Table 8 , updated the WIDD, added the maximum of RIDD and SIDD at 5 V and deleted RTI adder from stop with 32.768 kHz crystal external clock source reference enabled. Added maximum of I_{OLT} in Table 7 . |
| 3 | 12/4/2009 | Updated the part number information. |

Related Documentation

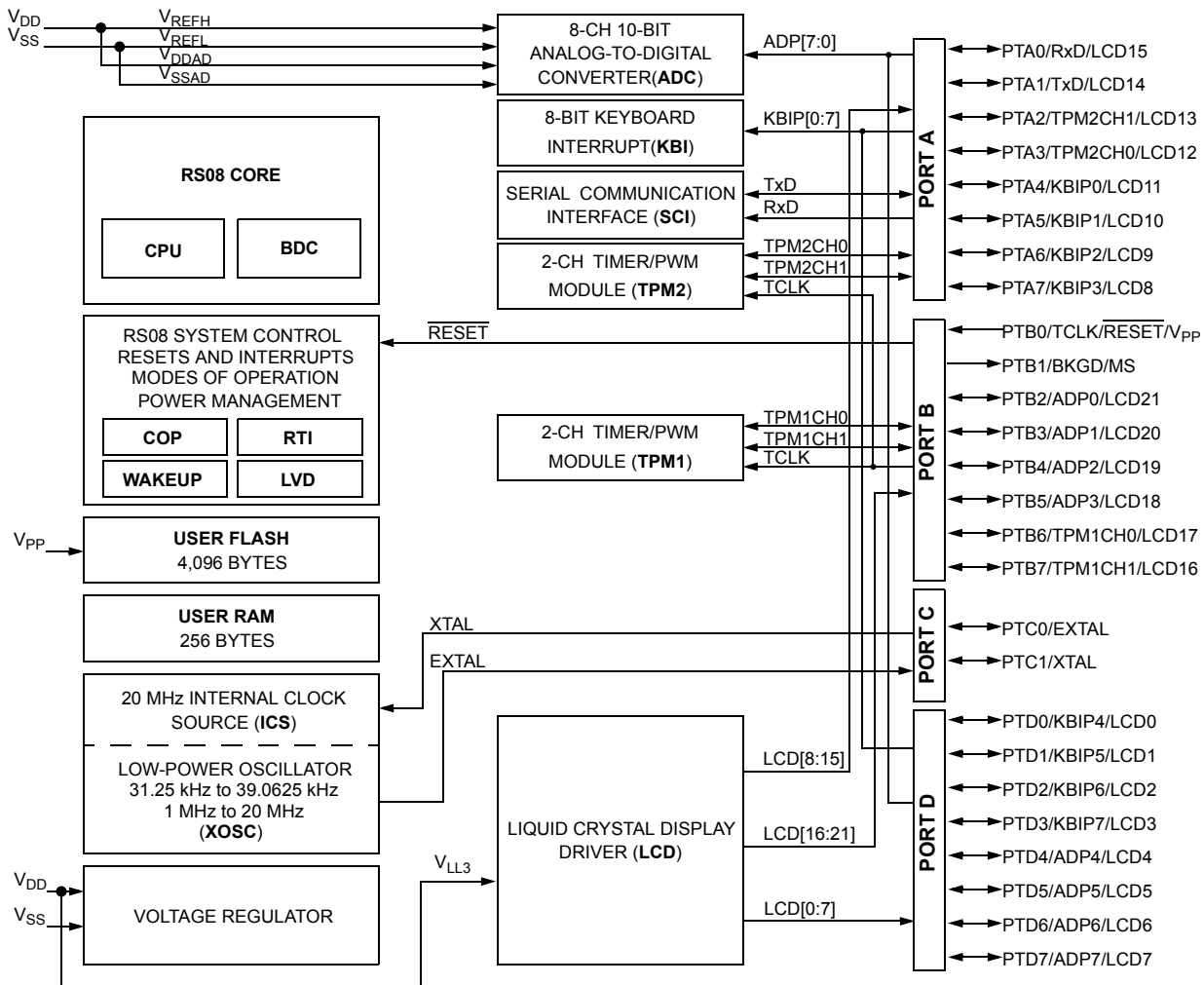
Find the most current versions of all documents at: <http://www.freescale.com>

Reference Manual (MC9RS08LE4RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, [Figure 1](#), shows the structure of the MC9RS08LE4 MCU.



NOTES:

1. PTB0/TCLK/RESET/V_{PP} is an input-only pin when used as port pin
2. PTB1/BKGD/MS is an output-only pin

Figure 1. MC9RS08LE4 Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9RS08LE4.

Table 2-1. Pin Availability by Package Pin-Count

| Pin Number | <-- Lowest Priority --> Highest | | | |
|------------|---------------------------------|-------|--------------|-----------------|
| | Port Pin | Alt 1 | Alt 2 | Alt 3 |
| 1 | PTD3 | | KBIP7 | LCD3 |
| 2 | PTD2 | | KBIP6 | LCD2 |
| 3 | PTD1 | | KBIP5 | LCD1 |
| 4 | PTD0 | | KBIP4 | LCD0 |
| 5 | | | | V _{DD} |
| 6 | | | | V _{SS} |
| 7 | PTC0 | | EXTAL | |
| 8 | PTC1 | | XTAL | |
| 9 | PTB0 | TCLK | <u>RESET</u> | V _{PP} |
| 10 | PTB1 | | BKGD | MS |
| 11 | PTB2 | | ADP0 | LCD21 |
| 12 | PTB3 | | ADP1 | LCD20 |
| 13 | PTB4 | | ADP2 | LCD19 |
| 14 | PTB5 | | ADP3 | LCD18 |
| 15 | PTB6 | | TPM1CH0 | LCD17 |
| 16 | PTB7 | | TPM1CH1 | LCD16 |
| 17 | PTA0 | | RxD | LCD15 |
| 18 | PTA1 | | TxD | LCD14 |
| 19 | PTA2 | | TPM2CH1 | LCD13 |
| 20 | PTA3 | | TPM2CH0 | LCD12 |
| 21 | PTA4 | | KBIP0 | LCD11 |
| 22 | PTA5 | | KBIP1 | LCD10 |
| 23 | PTA6 | | KBIP2 | LCD9 |
| 24 | PTA7 | | KBIP3 | LCD8 |
| 25 | PTD7 | | ADP7 | LCD7 |
| 26 | PTD6 | | ADP6 | LCD6 |
| 27 | PTD5 | | ADP5 | LCD5 |
| 28 | PTD4 | | ADP4 | LCD4 |

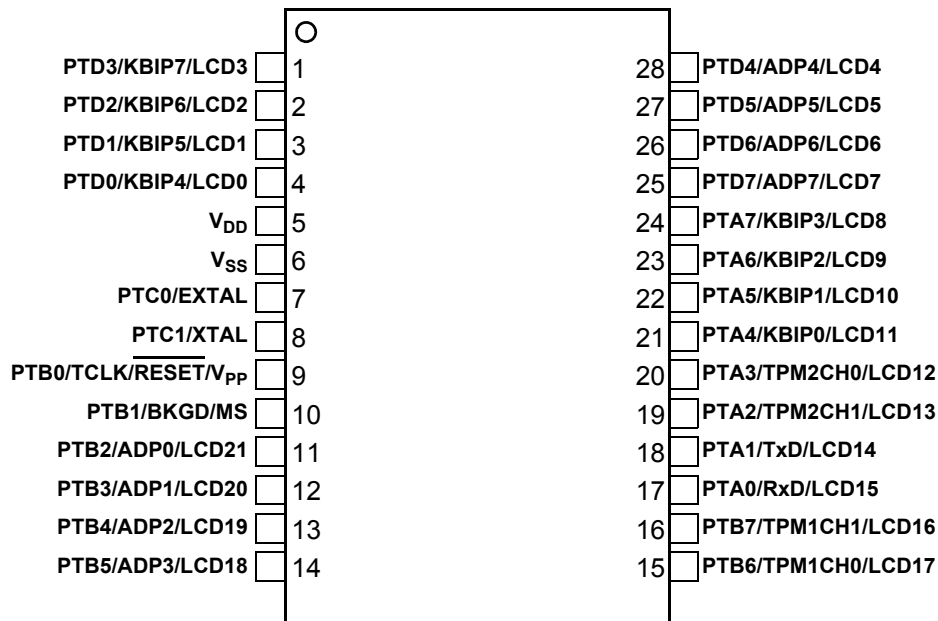


Figure 2. MC9RS08LE4 in 28-Pin SOIC Package

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9RS08LE4 microcontroller available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

| | |
|----------|--|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this chapter.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|-----------|------------------------|------|
| Supply voltage | V_{DD} | 2.7 to 5.5 | V |
| Maximum current into V_{DD} | I_{DD} | 120 | mA |
| Digital input voltage | V_{In} | -0.3 to $V_{DD} + 0.3$ | V |
| Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3} | I_D | ±25 | mA |
| Storage temperature range | T_{stg} | -55 to 150 | °C |

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the \overline{RESET}/V_{PP} pin which is internally clamped to V_{SS} only.

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits and it is user-determined rather than being controlled by the MCU design. In order to take PI/O into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

| Rating | Symbol | Value | Unit |
|--|---------------|-----------------------------|------|
| Operating temperature range (packaged) | T_A | T_L to T_H -40 to 85 | °C |
| Maximum junction temperature | T_{JMAX} | 105 | °C |
| Thermal resistance Single layer board 28-pin SOIC | θ_{JA} | 70 | °C/W |

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C /W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts chip internal power

$P_{I/O}$ = Power dissipation on input and output pins user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving [Equation 1](#) and [Equation 2](#) for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from [Equation 3](#) by measuring P_D (at equilibrium) for a known T_A . Using this value of K , the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A .

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device

DC Characteristics

specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

| Model | Description | Symbol | Value | Unit |
|------------|-----------------------------|--------|-------|----------|
| Human Body | Series resistance | R1 | 1500 | Ω |
| | Storage capacitance | C | 100 | pF |
| | Number of pulses per pin | — | 3 | — |
| Machine | Series resistance | R1 | 0 | Ω |
| | Storage capacitance | C | 200 | pF |
| | Number of pulses per pin | — | 3 | — |
| Latch-up | Minimum input voltage limit | — | -2.5 | V |
| | Maximum input voltage limit | — | 7.5 | V |

Table 6. ESD and Latch-Up Protection Characteristics

| No. | Rating ¹ | Symbol | Min | Max | Unit |
|-----|--|-----------|-------------|-----|------|
| 1 | Human body model (HBM) | V_{HBM} | ± 2000 | — | V |
| 2 | Machine model (MM) | V_{MM} | ± 200 | — | V |
| 3 | Charge device model (CDM) | V_{CDM} | ± 500 | — | V |
| 4 | Latch-up current at $T_A = 85^\circ\text{C}$ | I_{LAT} | $\pm 100^2$ | — | mA |
| | Latch-up current at $T_A = 85^\circ\text{C}$ | I_{LAT} | $\pm 75^3$ | — | mA |

¹ Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

² These pins meet JESD78A Class II (section 1.2) Level A (section 1.3) requirement of ± 100 mA.

³ This pin meets JESD78A Class II (section 1.2) Level B (section 1.3) characterization to ± 75 mA.

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 7. DC Characteristics (Temperature Range = -40 to 85°C Ambient)

| Num | C | Parameter | Symbol | Min | Typical | Max | Unit |
|-----|---|--|-----------|----------------------|--------------|--------------|------|
| 1 | | Supply voltage (run, wait and stop modes.) $0 < f_{Bus} < 10\text{MHz}$ | V_{DD} | 2.7 | — | 5.5 | — |
| 2 | C | Minimum RAM retention supply voltage applied to V_{DD} | V_{RAM} | 0.8^1 | — | — | V |
| 3 | P | Low-voltage Detection threshold (V_{DD} falling) (V_{DD} rising) | V_{LVD} | 1.80 1.88 | 1.86 1.94 | 1.95 2.03 | V |
| 4 | C | Power on RESET (POR) voltage | V_{POR} | 0.9 | — | 1.7 | V |
| 5 | C | Input high voltage ($V_{DD} > 2.3\text{V}$) (all digital inputs) | V_{IH} | $0.70 \times V_{DD}$ | — | — | V |
| | | Input high voltage ($1.8\text{V} \leq V_{DD} \leq 2.3\text{V}$) (all digital inputs) | | $0.85 \times V_{DD}$ | — | — | V |

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

| Num | C | Parameter | Symbol | Min | Typical | Max | Unit |
|-----|---|--|-------------|----------------------|---------|----------------------|------------------|
| 6 | C | Input low voltage ($V_{DD} > 2.3$ V) (all digital inputs) | V_{IL} | — | — | $0.30 \times V_{DD}$ | V |
| | | Input low voltage ($1.8 \text{ V} \leq V_{DD} \leq 2.3$ V) (all digital inputs) | | — | — | $0.30 \times V_{DD}$ | V |
| 7 | C | Input hysteresis (all digital inputs) | V_{hys} | $0.06 \times V_{DD}$ | — | — | V |
| 8 | P | Input leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS} , all input only pins | $ I_{In} $ | — | 0.025 | 1.0 | μA |
| 9 | P | High impedance (off-state) leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS} , all input/output | $ I_{OZ} $ | — | 0.025 | 1.0 | μA |
| 10 | P | Internal pullup/pulldown resistors ² (all port pins) | R_{PU} | 20 | 45 | 65 | $\text{k}\Omega$ |
| 11 | C | Output high voltage (port A) $I_{OH} = -5$ mA ($V_{DD} \geq 4.5$ V) | V_{OH} | $V_{DD} - 0.8$ | — | — | V |
| | | $I_{OH} = -3$ mA ($V_{DD} \geq 3$ V) | | | — | — | |
| | | $I_{OH} = -2$ mA ($V_{DD} \geq 1.8$ V) | | | — | — | |
| 12 | C | Maximum total I_{OH} for all port pins | $ I_{OHT} $ | — | — | 40 | mA |
| 13 | C | Output low voltage (port A) $I_{OL} = 5$ mA ($V_{DD} \geq 4.5$ V) | V_{OL} | — | — | 0.8 | V |
| | | $I_{OL} = 3$ mA ($V_{DD} \geq 3$ V) | | — | — | 0.8 | |
| | | $I_{OL} = 2$ mA ($V_{DD} \geq 1.8$ V) | | — | — | 0.8 | |
| 14 | C | Maximum total I_{OL} for all port pins | I_{OLT} | — | — | 100 | mA |
| 15 | C | dc injection current ^{3, 4, 5, 6} $V_{In} < V_{SS}$, $V_{In} > V_{DD}$ Single pin limit | — | — | — | 0.2 | mA |
| | | Total MCU limit, includes sum of all stressed pins | — | — | — | 0.8 | mA |
| 16 | C | Input capacitance (all non-supply pins) | C_{In} | — | — | 7 | pF |

¹ This parameter is characterized and not tested on each device.

² Measurement condition for pull resistors: $V_{In} = V_{SS}$ for pullup and $V_{In} = V_{DD}$ for pulldown.

³ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{\text{RESET}}/V_{PP}$ which is internally clamped to V_{SS} only

⁴ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁵ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁶ This parameter is characterized and not tested on each device.

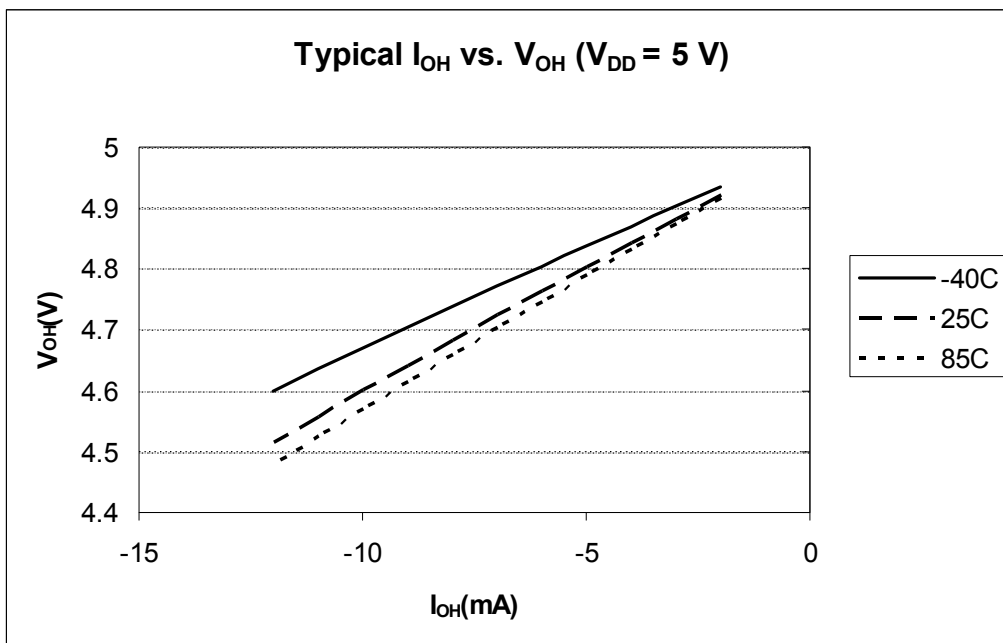


Figure 3. Typical I_{OH} vs. V_{OH} ($V_{DD} = 5\text{ V}$)

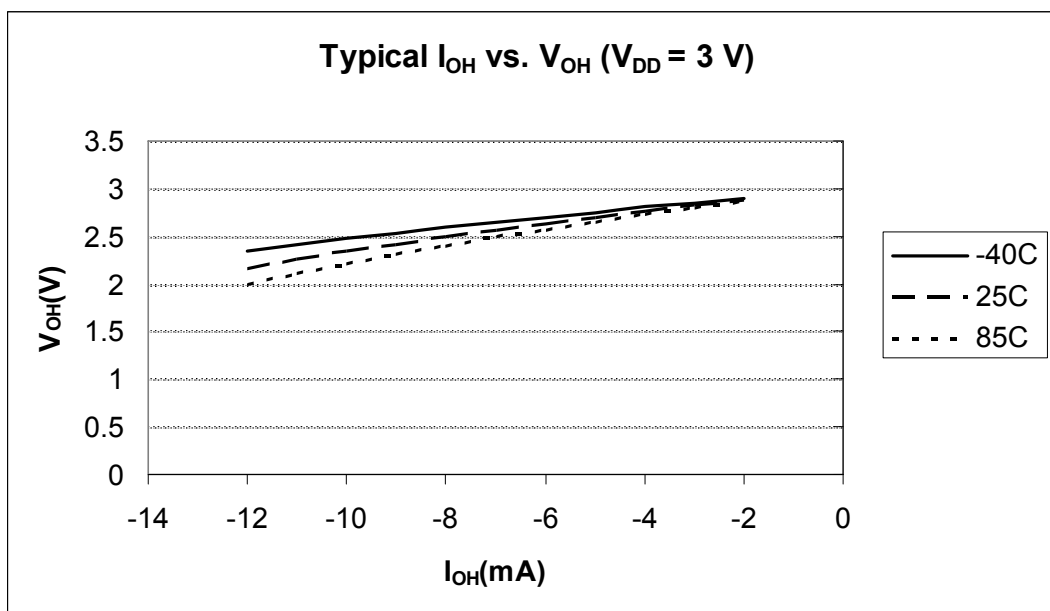


Figure 4. Typical I_{OH} vs. V_{OH} ($V_{DD} = 3\text{ V}$)

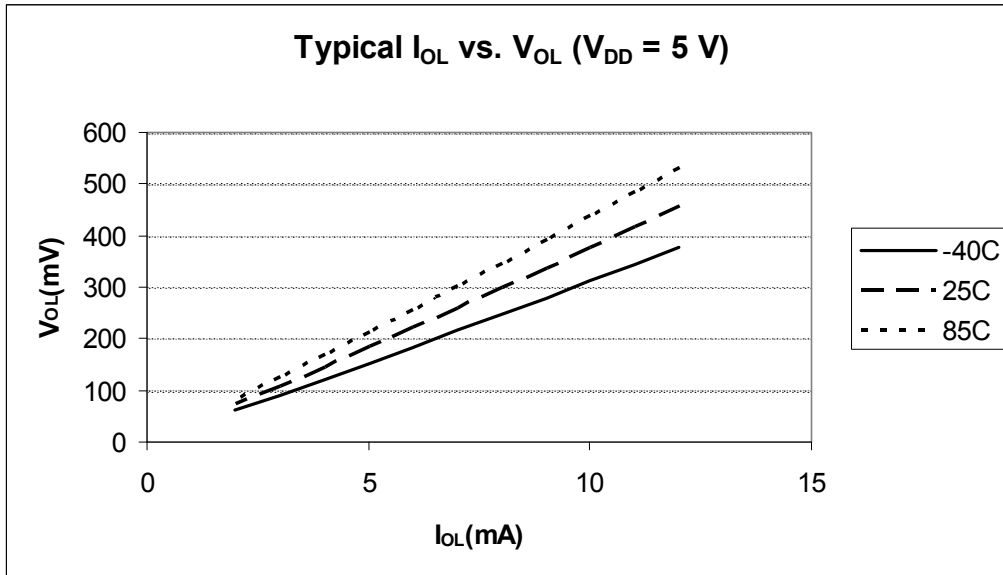


Figure 5. Typical I_{OL} vs. V_{OL} ($V_{DD} = 5\text{ V}$)

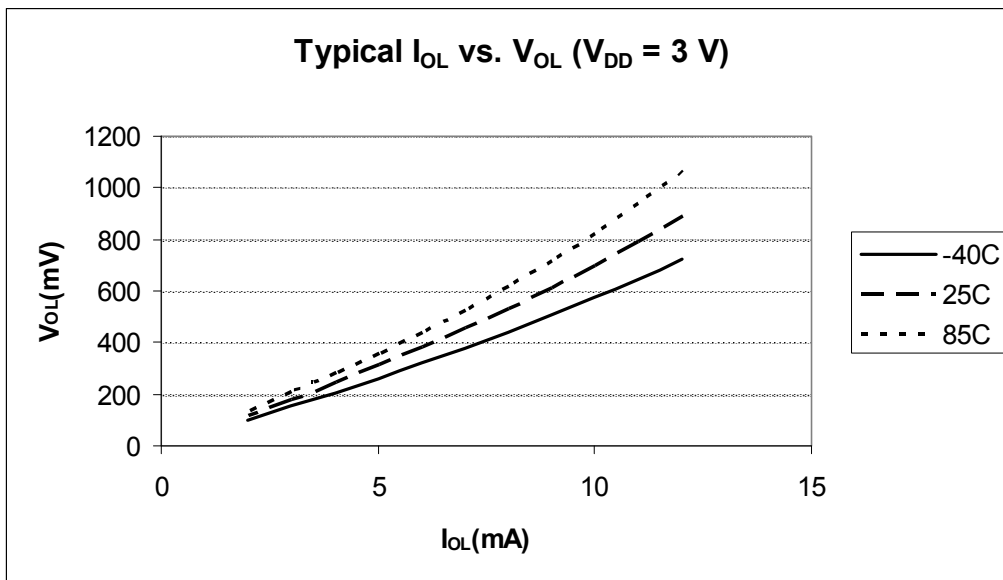


Figure 6. Typical I_{OL} vs. V_{OL} ($V_{DD} = 3\text{ V}$)

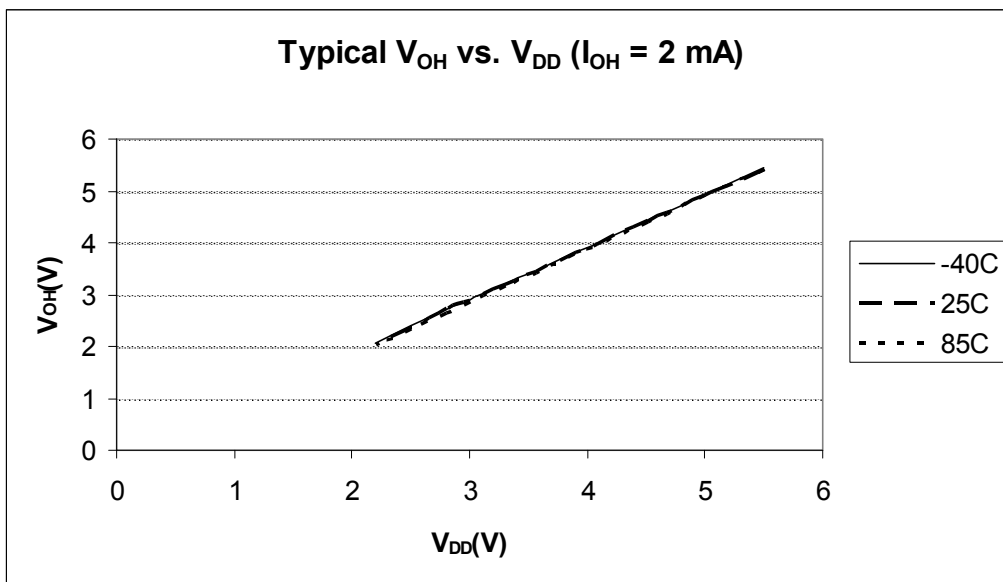


Figure 7. Typical V_{OH} vs. V_{DD} ($I_{OH} = 2 \text{ mA}$)

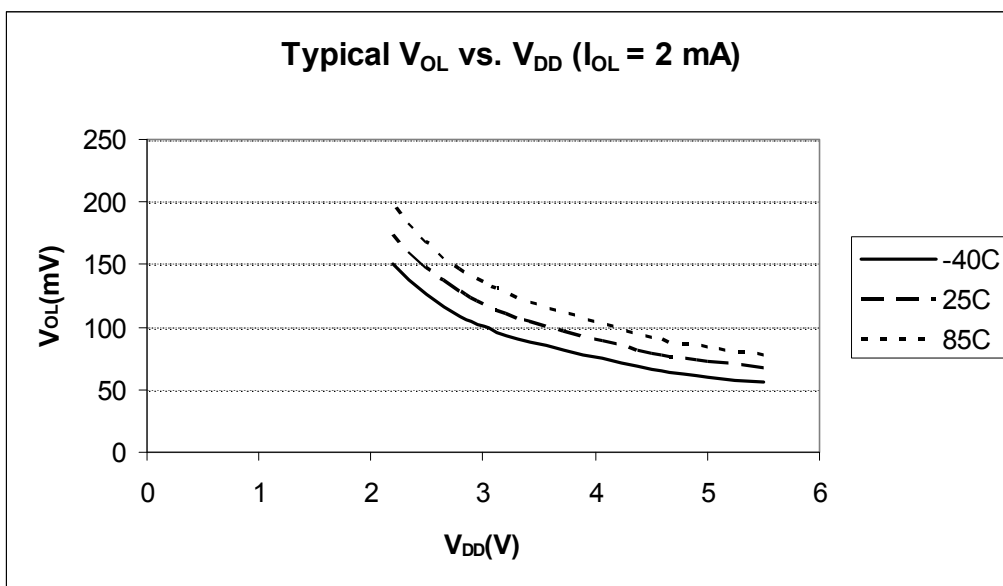


Figure 8. Typical V_{OL} vs. V_{DD} ($I_{OL} = 2 \text{ mA}$)

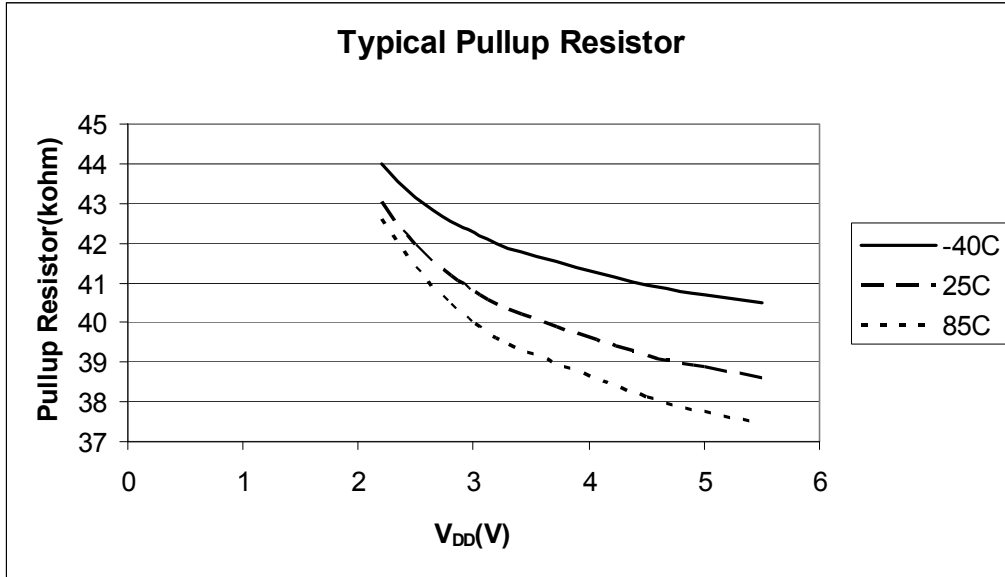


Figure 9. Typical Pullup Resistor

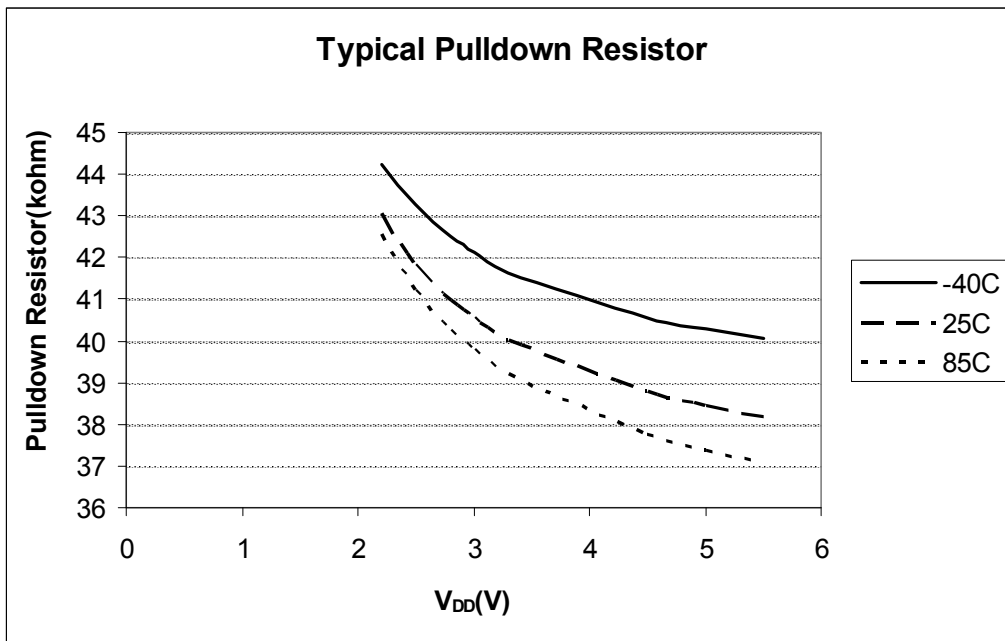


Figure 10. Typical Pulldown Resistor

3.7 Supply Current Characteristics

Table 8. Supply Current Characteristics

| Num | C | Parameter | Symbol | Bus Freq. (MHz) | V _{DD} (V) | Temp. (°C) | Typical | Max ¹ | Unit |
|-----|---|---|--------|-----------------|---------------------|-----------------|----------------------------|------------------|------|
| 1 | P | Run supply current ² | RIDD | 10 | 5 | -40 25 85 | 3.78 3.81 3.83 | 20 | mA |
| | C | | | | 3 | -40 25 85 | 3.70 3.76 3.77 | — | |
| | T | | | 1.25 | 5 | -40 25 85 | 0.94 0.95 0.95 | — — — | |
| | T | | | | 3 | -40 25 85 | 0.94 0.94 0.94 | — — — | |
| 2 | T | Wait supply current ² | WIDD | 2 | 5 | -40 25 85 | 932 943 947 | — — — | μA |
| | T | | | | 3 | -40 25 85 | 940 959 954 | — — — | |
| | T | | | 1 | 5 | -40 25 85 | 712 714 717 | — — — | |
| | T | | | | 3 | -40 25 85 | 718 716 715 | — — — | |
| 3 | P | Stop mode supply current | SIDD | — | 5 | -40 25 85 | 1.14 1.43 3.75 | 15 | μA |
| | C | | | | 3 | -40 25 85 | 0.61 0.88 2.96 | — — — | |
| 4 | T | ADC adder to stop ³ | — | — | 5 | -40 25 85 | 119.85 128.72 131.70 | — — — | μA |
| | T | | | | 3 | -40 25 85 | 115.28 123.86 126.60 | — — — | |
| 5 | T | RTI adder from stop with 1 kHz clock source enabled | — | — | 5 | -40 25 85 | 0.10 0.11 0.12 | — — — | μA |
| | T | | | | 3 | -40 25 85 | 0.11 0.11 0.12 | — — — | |

Table 8. Supply Current Characteristics (continued)

| Num | C | Parameter | Symbol | Bus Freq. (MHz) | V _{DD} (V) | Temp. (°C) | Typical | Max ¹ | Unit |
|-----|---|--|--------|-----------------|---------------------|------------|---------|------------------|------|
| 6 | T | LVI adder from stop (LVDE = 1 and LVDSE = 1) | — | — | 5 | -40 | 69.40 | — | μA |
| | | | | | | 25 | 72.07 | — | |
| | | | | | | 85 | 73.29 | — | |
| | T | | | — | 3 | -40 | 69.74 | — | |
| | | | | | | 25 | 72.19 | — | |
| | | | | | | 85 | 72.67 | — | |

¹ Maximum value is measured at the nominal V_{DD} voltage times 10% tolerance. Values given here are preliminary estimates prior to completing characterization

² Does not include any dc loads on port pins

³ Required asynchronous ADC clock and LVD to be enabled.

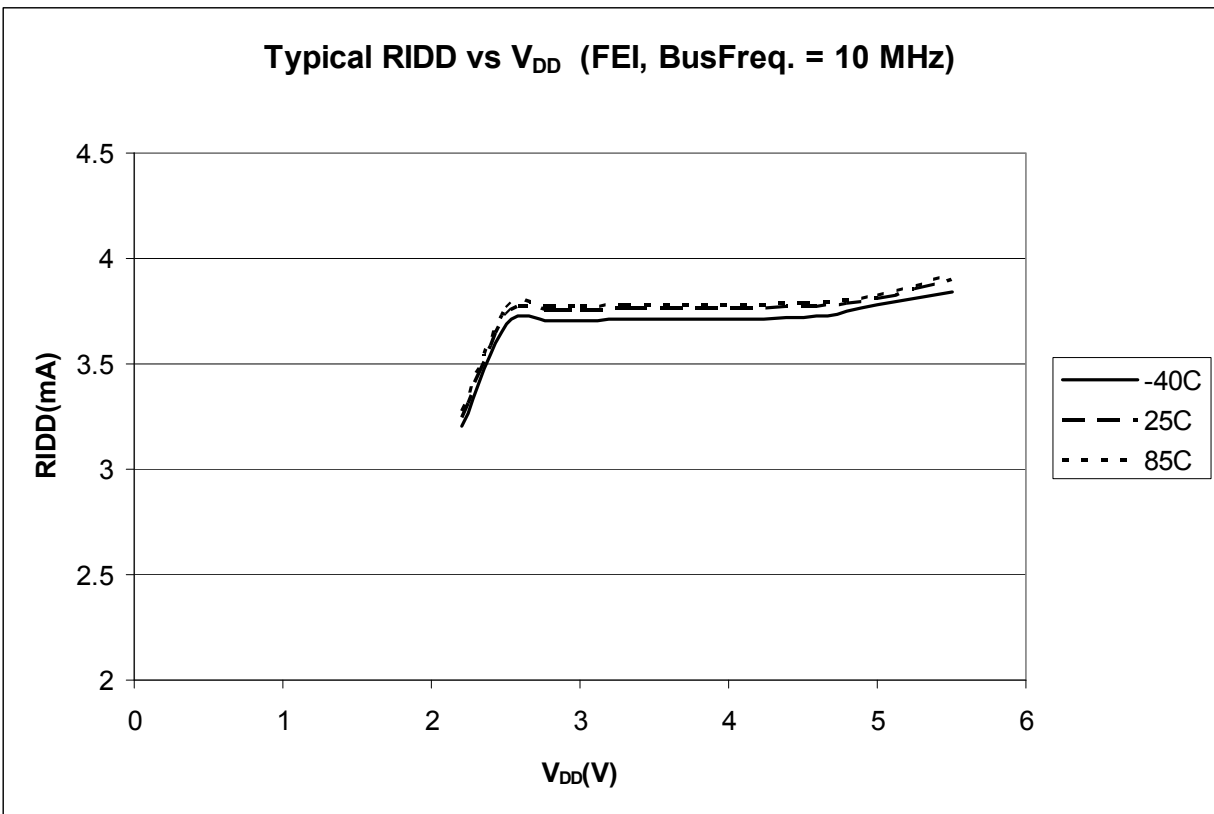


Figure 11. Typical RIDD vs. V_{DD} (FEI, BusFreq. = 10 MHz)

3.8 External Oscillator (XOSC) Characteristics

Refer to [Figure 12](#) for crystal or resonator circuit.

Table 9. External Oscillator Specifications (Temperature Range = -40 to 85°C Ambient)

| Num | C | Characteristic | Symbol | Min | Typical ¹ | Max | Unit |
|---------------------|---|--|--------------------------|-----------------------|----------------------|--------|------|
| 1 | D | Oscillator crystal or resonator (EREFS = 1) | | | | | |
| | | Low range, (IREFS = x) | f_{lo} | 32 | — | 38.4 | kHz |
| | | High range, FLL bypassed external (CLKS = 10, IREFS = x) | f_{hi_byp} | 1 | — | 5 | MHz |
| | | High range, FLL engaged external (CLKS = 00, IREFS = 0) | f_{hi_eng} | 1 | — | 5 | MHz |
| 2 | D | Load capacitors | C_1 C_2 | See Note ² | | | |
| 3 | D | Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz) | R_F | | 10 1 | | MΩ |
| 4 | D | Series resistor | R_S | | | | kΩ |
| | | Low range | | | | | |
| | | Low Gain (HGO = 0) | | — | 0 | — | |
| | | High Gain (HGO = 1) | | — | 100 | — | |
| | | High range | | | | | |
| Low Gain (HGO = 0) | — | 0 | — | | | | |
| High Gain (HGO = 1) | — | 0 | — | | | | |
| ≥ 8 MHz | — | 0 | — | | | | |
| 4 MHz | — | 10 | — | | | | |
| 1 MHz | — | 20 | — | | | | |
| 5 | D | Crystal start-up time ^{3,4} Low range High range | t_{CSTL} t_{CSTH} | — — | 500 4 | — — | ms |

¹ Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

² See crystal or resonator manufacturer’s recommendation.

³ This parameter is characterized and not tested on each device.

⁴ Proper PC board layout procedures must be followed to achieve specifications.

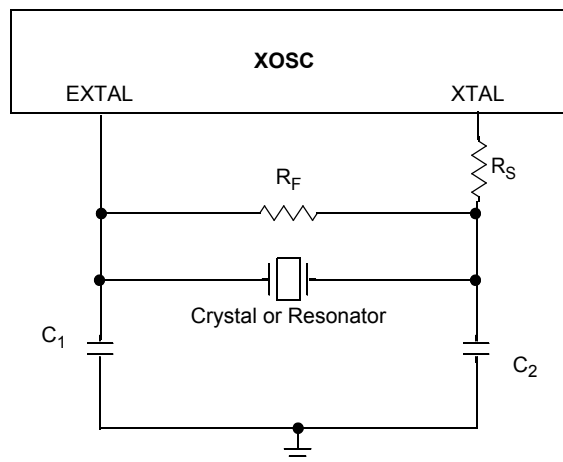


Figure 12. Typical Crystal or Resonator Circuit

3.9 Internal Clock Source (ICS) Characteristics

Table 10. ICS Frequency Specifications (Temperature Range = -40 to 85°C Ambient)

| Num | C | Characteristic | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|--|---------------------------------|--------------|----------------------|---------|--------------------|
| 1 | C | Square wave input clock frequency (EREFS = 0) FLL bypass external (CLKS = 10) FLL engaged external (CLKS = 00) | f_{extal} | 0 0.03125 | — — | 20 5 | MHz |
| 2 | C | Average internal reference frequency - untrimmed | $f_{\text{int_ut}}$ | 25 | 31.25 | 41.66 | kHz |
| 3 | C | Average internal reference frequency - trimmed | $f_{\text{int_t}}$ | 31.25 | 31.25 | 39.0625 | kHz |
| 4 | C | DCO output frequency range — untrimmed | $f_{\text{dco_ut}}$ | 12.8 | 16 | 21.33 | MHz |
| 5 | C | DCO output frequency range — trimmed | $f_{\text{dco_t}}$ | 16 | 16 | 20 | MHz |
| 6 | C | Resolution of trimmed DCO output frequency at fixed voltage and temperature | $\Delta f_{\text{dco_res_t}}$ | — | — | ±0.2 | % f_{dco} |
| 7 | C | Total deviation of trimmed DCO output frequency over voltage and temperature | $\Delta f_{\text{dco_t}}$ | — | — | ±2 | % f_{dco} |
| 8 | C | FLL acquisition time ^{3,2} | t_{acquire} | — | — | 1 | ms |
| 9 | C | Long term Jitter ³ of DCO output clock (averaged over 2 ms interval) | C_{Jitter} | — | — | 0.6 | % f_{dco} |

¹ Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

² This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

³ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

3.10 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 11. Control Timing

| Num | C | Parameter | Symbol | Min | Typical | Max | Unit |
|-----|---|--|------------------------------------|----------------------|----------|--------|------|
| 1 | D | Bus frequency ($t_{\text{cyc}} = 1/f_{\text{Bus}}$) | f_{Bus} | 0 | — | 10 | MHz |
| 2 | D | Real time interrupt internal oscillator period | t_{RTI} | 700 | 1000 | 1300 | μs |
| 3 | D | External $\overline{\text{RESET}}$ pulse width ¹ | t_{extrst} | 150 | — | — | ns |
| 4 | D | KBI pulse width ² | t_{KBIPW} | $1.5 t_{\text{cyc}}$ | — | — | ns |
| 5 | D | KBI pulse width in stop ¹ | t_{KBIPWS} | 100 | — | — | ns |
| 6 | C | Port rise and fall time (load = 50 pF) ³ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1) | $t_{\text{Rise}}, t_{\text{Fall}}$ | — — | 11 35 | — — | ns |

¹ This is the shortest pulse that is guaranteed to pass through the pin input filter circuitry. Shorter pulses may or may not be recognized.

AC Characteristics

- 2 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- 3 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$.

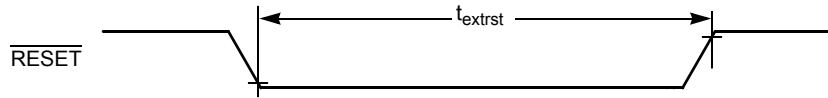


Figure 13. Reset Timing

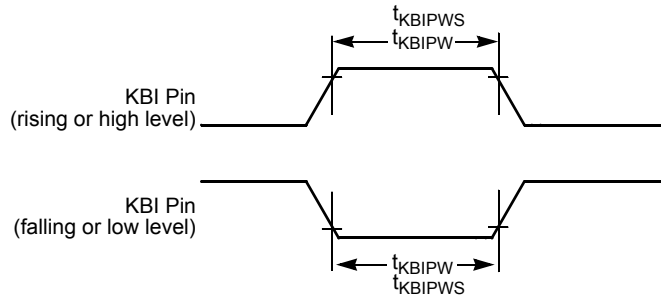


Figure 14. KBI Pulse Width

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 12. TPM/MTIM Input Timing

| Num | C | Function | Symbol | Min | Max | Unit |
|-----|---|---------------------------|------------|-----|-------------|-----------|
| 1 | D | External clock frequency | f_{TCLK} | 0 | $f_{Bus}/4$ | MHz |
| 2 | D | External clock period | t_{TCLK} | 4 | — | t_{CYC} |
| 3 | D | External clock high time | t_{clkh} | 1.5 | — | t_{CYC} |
| 4 | D | External clock low time | t_{clkl} | 1.5 | — | t_{CYC} |
| 5 | D | Input capture pulse width | f_{ICPW} | 1.5 | — | t_{CYC} |

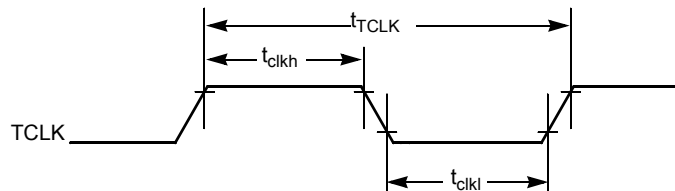


Figure 15. Timer External Clock

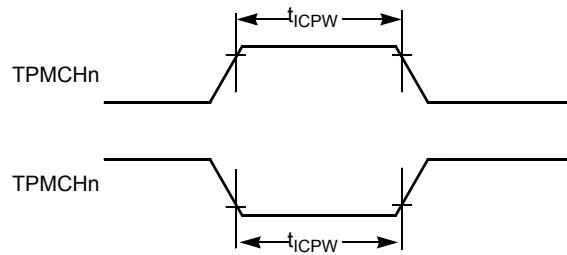


Figure 16. Timer Input Capture Pulse

3.11 ADC Characteristics

Figure 17. 5 Volt 10-bit ADC Operating Conditions

| Characteristic | Conditions | Symb | Min | Typical ¹ | Max | Unit |
|--|---|-------------------|------------|----------------------|------------|------------|
| Supply voltage | Absolute | V_{DDAD} | 1.8 | — | 5.5 | V |
| | Delta to V_{DD} ($V_{DD} - V_{DDAD}$) ² | ΔV_{DDAD} | -100 | 0 | 100 | mV |
| Ground voltage | Delta to V_{SS} ($V_{SS} - V_{SSAD}$) ² | ΔV_{SSAD} | -100 | 0 | 100 | mV |
| Reference voltage high | | V_{REFH} | 1.8 | V_{DDAD} | V_{DDAD} | V |
| Reference voltage low | | V_{REFL} | V_{SSAD} | V_{SSAD} | V_{SSAD} | V |
| Input voltage | | V_{ADIN} | V_{REFL} | — | V_{REFH} | V |
| Input capacitance | | C_{ADIN} | — | 4.5 | 5.5 | pF |
| Input resistance | | R_{ADIN} | — | 3 | 5 | k Ω |
| Analog source resistance external to MCU | 10 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$ | R_{AS} | — | — | 5 | k Ω |
| | 8 bit mode (all valid f_{ADCK}) | | — | — | 10 | |
| ADC conversion clock frequency | High speed (ADLPC = 0) | f_{ADCK} | 0.4 | — | 8.0 | MHz |
| | Low power (ADLPC = 1) | | 0.4 | — | 4.0 | |

¹ Typical values assume $V_{DDAD} = 5.0\text{ V}$, Temp = 25 °C, $f_{ADCK} = 1.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential difference.

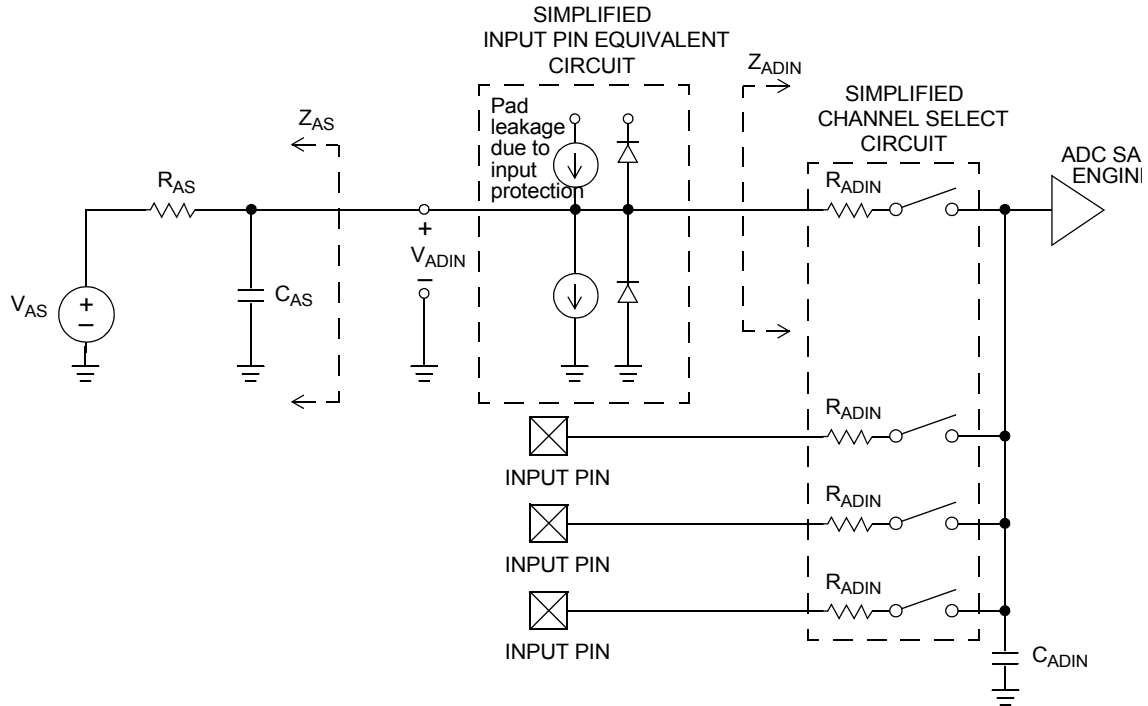


Figure 18. ADC Input Impedance Equivalency Diagram

Table 13. 10-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

| Num | C | Characteristic | Conditions | Symb | Min | Typical ¹ | Max | Unit |
|-----|---|---|-------------------------|-------------|------|----------------------|-----|---------|
| 1 | T | Supply current ADLPC=1 ADLSMP=1 ADCO=1 | | I_{DDAD} | — | 133 | — | μA |
| 2 | T | Supply current ADLPC=1 ADLSMP=0 ADCO=1 | | I_{DDAD} | — | 218 | — | μA |
| 3 | T | Supply current ADLPC=0 ADLSMP=1 ADCO=1 | | I_{DDAD} | — | 327 | — | μA |
| 4 | P | Supply current ADLPC=0 ADLSMP=0 ADCO=1 | $V_{DDAD} \leq 5.5 V$ | I_{DDAD} | — | 0.582 | 1 | mA |
| 5 | | Supply current | Stop, reset, module off | I_{DDAD} | — | 0.011 | 1 | μA |
| 6 | P | ADC asynchronous clock source | High speed (ADLPC = 0) | f_{ADACK} | 2 | 3.3 | 5 | MHz |
| | | | Low power (ADLPC = 1) | | 1.25 | 2 | 3.3 | |

Table 13. 10-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$) (continued)

| Num | C | Characteristic | Conditions | Symb | Min | Typical ¹ | Max | Unit |
|-----|---|--|--|-----------|-----|----------------------|-----------|------------------|
| 7 | P | Conversion time (Including sample time) | Short sample (ADLSMP = 0) | t_{ADC} | — | 20 | — | ADCK cycles |
| | | | Long sample (ADLSMP = 1) | | — | 40 | — | |
| 8 | P | Sample time | Short sample (ADLSMP = 0) | t_{ADS} | — | 3.5 | — | ADCK cycles |
| | | | Long sample (ADLSMP = 1) | | — | 23.5 | — | |
| 9 | P | Total unadjusted error | 10-bit mode | E_{TUE} | — | ± 1 | ± 2.5 | LSB ² |
| | | | 8-bit mode | | — | ± 0.5 | ± 1.0 | |
| 10 | P | Differential non-linearity | 10-bit mode | DNL | — | ± 0.5 | ± 1.0 | LSB ² |
| | | | 8-bit mode | | — | ± 0.3 | ± 0.5 | |
| | | | Monotonicity and no-missing-codes guaranteed | | | | | |
| 11 | C | Integral non-linearity | 10-bit mode | INL | — | ± 0.5 | ± 1.0 | LSB ² |
| | | | 8-bit mode | | — | ± 0.3 | ± 0.5 | |
| 12 | P | Zero-scale error | 10-bit mode | E_{ZS} | — | ± 0.5 | ± 1.5 | LSB ² |
| | | | 8-bit mode | | — | ± 0.5 | ± 0.5 | |
| 13 | P | Full-scale error $V_{ADIN} = V_{DDA}$ | 10-bit mode | E_{FS} | — | ± 0.5 | ± 1.5 | LSB ² |
| | | | 8-bit mode | | — | ± 0.5 | ± 0.5 | |
| 14 | D | Quantization error | 10-bit mode | E_Q | — | — | ± 0.5 | LSB ² |
| | | | 8-bit mode | | — | — | ± 0.5 | |
| 15 | D | Input leakage error pad leakage ³ * R_{AS} | 10 bit mode | E_{IL} | — | ± 0.2 | ± 2.5 | LSB ² |
| | | | 8 bit mode | | — | ± 0.1 | ± 1 | |

¹ Typical values assume $V_{DDAD} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

³ Based on input pad leakage current. Refer to pad electrical.

3.12 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. For detailed information about program/erase operations, see the reference manual.

Table 14. Flash Characteristics

| Num | C | Characteristic | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|----------------------------------|----------|------|----------------------|------|------|
| 1 | D | Supply voltage for program/erase | V_{DD} | 2.7 | — | 5.5 | V |
| 2 | D | Program/Erase voltage | V_{PP} | 11.8 | 12 | 12.2 | V |

Table 14. Flash Characteristics (continued)

| Num | C | Characteristic | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|--|---|--------|----------------------|------------|----------|
| 3 | C | V _{PP} current Program Mass erase | I _{VPP_prog} I _{VPP_erase} | — — | — — | 200 100 | μA μA |
| 4 | D | Supply voltage for read operation 0 < f _{Bus} < 10 MHz | V _{Read} | 1.8 | — | 5.5 | V |
| 5 | P | Byte program time | t _{prog} | 20 | — | 40 | μs |
| 6 | P | Mass erase time | t _{me} | 500 | — | — | ms |
| 7 | C | Cumulative program HV time ² | t _{hv} | — | — | 8 | ms |
| 8 | C | Total cumulative HV time (total of t _{me} & t _{hv} applied to device) | t _{hv_total} | — | — | 2 | hours |
| 9 | D | HVEN to program setup time | t _{pgs} | 10 | — | — | μs |
| 10 | D | PGM/MASS to HVEN setup time | t _{nvs} | 5 | — | — | μs |
| 11 | D | HVEN hold time for PGM | t _{nvh} | 5 | — | — | μs |
| 12 | D | HVEN hold time for MASS | t _{nvh1} | 100 | — | — | μs |
| 13 | D | V _{PP} to PGM/MASS setup time | t _{vps} | 20 | — | — | ns |
| 14 | D | HVEN to V _{PP} hold time | t _{vph} | 20 | — | — | ns |
| 15 | D | V _{PP} rise time ³ | t _{vrs} | 200 | — | — | ns |
| 16 | D | Recovery time | t _{rcv} | 1 | — | — | μs |
| 17 | D | Program/erase endurance T _L to T _H = -40°C to 85°C | — | 1000 | — | — | cycles |
| 18 | C | Data retention | t _{D_ret} | 100 | — | — | years |

¹ Typicals are measured at 25 °C.

² t_{hv} is the cumulative high voltage programming time to the same row before next erase. Same address can not be programmed more than twice before next erase.

³ Fast V_{PP} rise time may potentially trigger the ESD protection structure, which may result in over-current flowing into the pad and cause permanent damage to the pad. External filtering for the V_{PP} power source is recommended. An example V_{PP} filter is shown in [Figure 19](#).

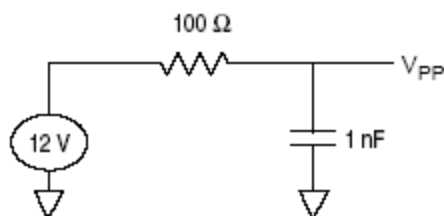
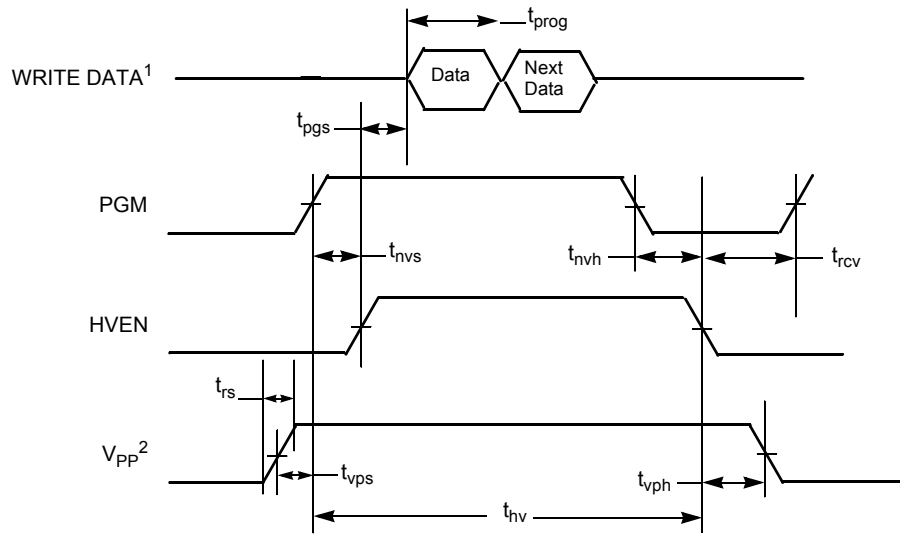
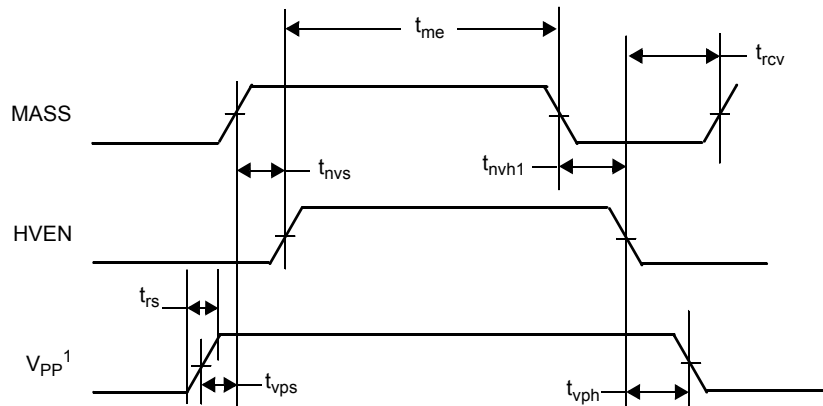


Figure 19. Example V_{PP} Filtering



- ¹ Next Data applies if programming multiple bytes in a single row, refer to *MC9RS08LE4 Reference Manual*.
- ² V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 20. Flash Program Timing



- ¹ V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

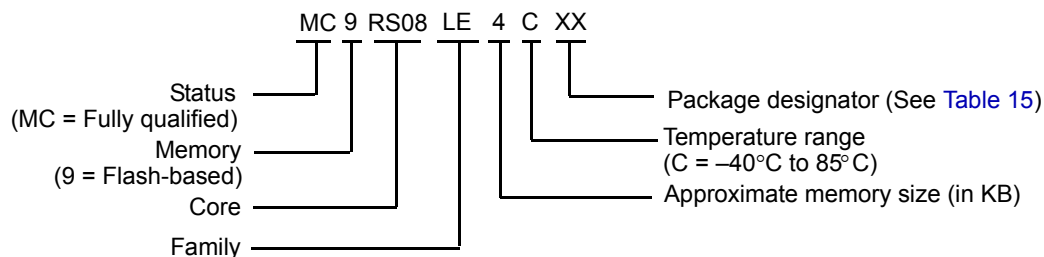
Figure 21. Flash Mass Erase Timing

4 Ordering Information

This section contains ordering numbers for MC9RS08LE4 devices. See below for an example of the device numbering system.

Table 15. Device Numbering System

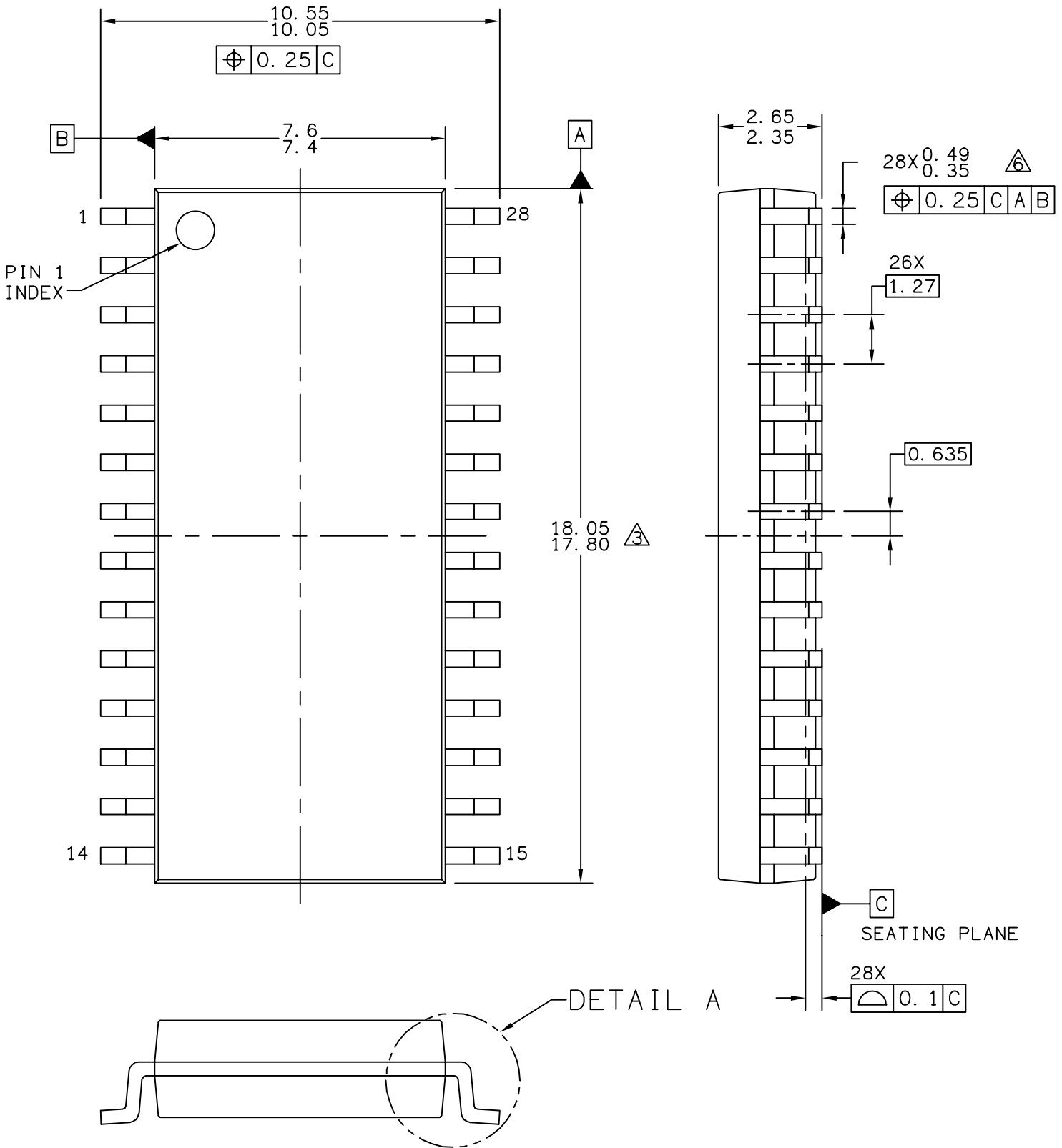
| Device Number | Memory | | Package | | |
|-------------------|--------|-----------|---------|------------|--------------|
| | Flash | RAM | Type | Designator | Document No. |
| MC9RS08LE4 | 4 KB | 256 bytes | 28 SOIC | WL | 98ASB42345B |



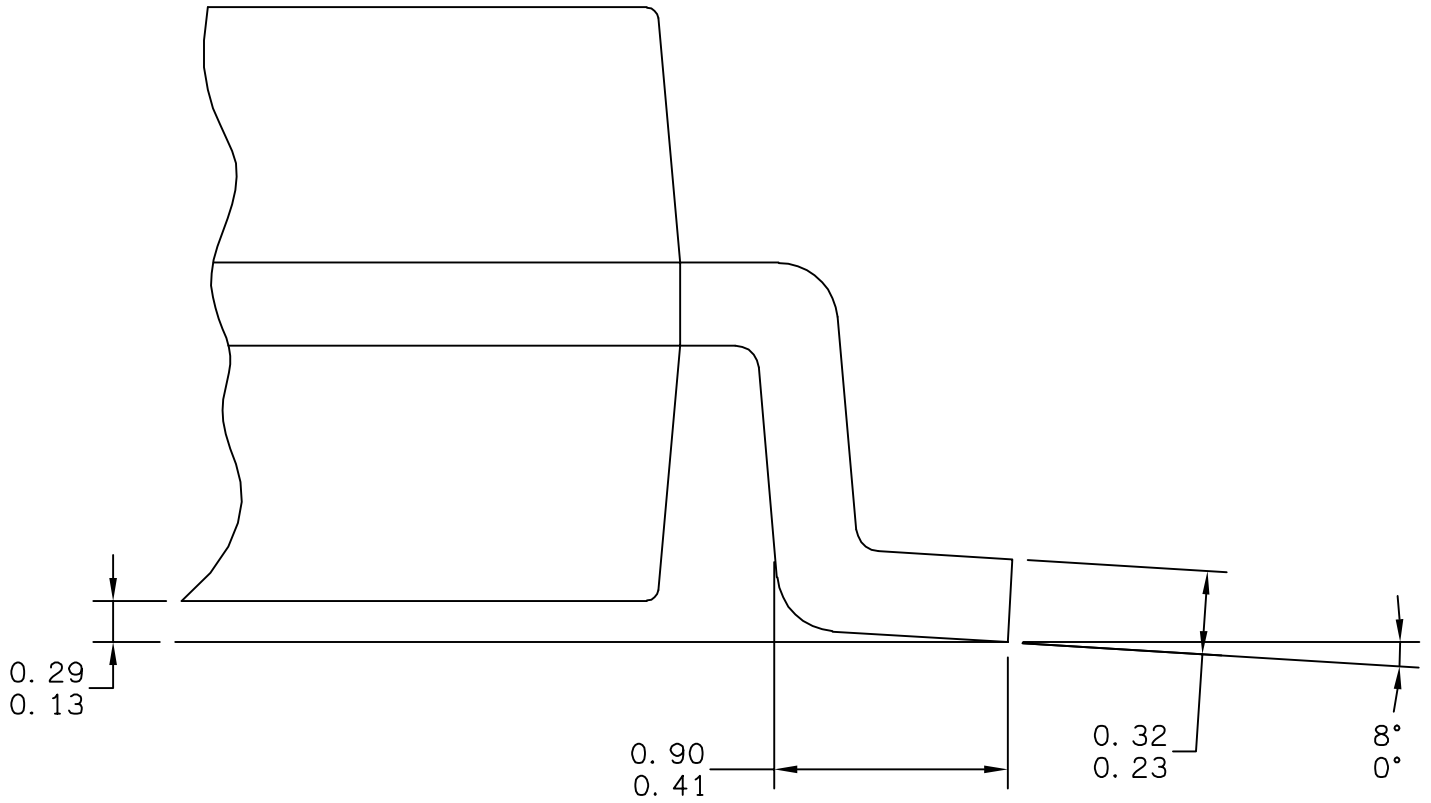
5 Mechanical Drawings

The following pages contain mechanical specifications for MC9RS08LE4 package options.

- 28-pin SOIC (small outline integrated circuit)



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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

4. 751F-01 THRU -04 OBSOLETE. NEW STANDARD: 751F-05

5. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

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