# SNx4LV74A Dual Positive-Edge-Triggered D-Type Flip-Flops

## 1 Features

- 2-V to 5.5-V $V_{CC}$ Operation
- Maximum $t_{pd}$ of 8.5 ns at 5 V
- Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) > 2.3 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$ Supports Partial-Power-Down Mode Operation
- Latch-up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 500-V Charged-Device Model (C101)

## 2 Applications

- Programmable Logic Controller (PLC)
- DCS and PAC: Analog Input Module
- AV Receiver
- Server PSU
- STB, DVR, and Streaming Media (Withdraw)
- Server Motherboard

## 3 Description

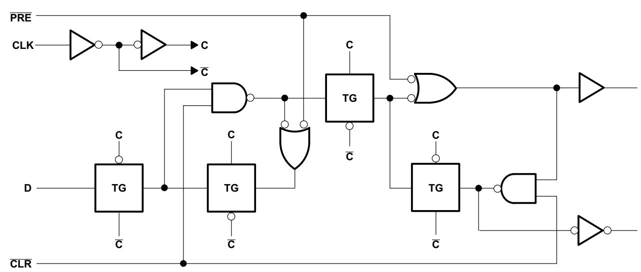
These dual positive-edge-triggered D-type flip-flops are designed for 2-V to 5.5-V $V_{CC}$ operation.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LV74A | VQFN (14) | 3.50 mm × 3.50 mm |
| | SOIC (14) | 8.65 mm × 3.91 mm |
| | SOP (14) | 10.30 mm × 5.30 mm |
| | SSOP (14) | 6.20 mm × 5.30 mm |
| | TSSOP (14) | 5.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram, Each Flip-Flop (Positive Logic)**



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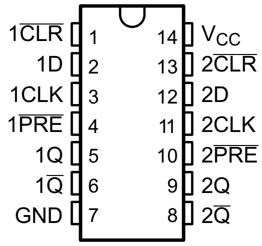
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

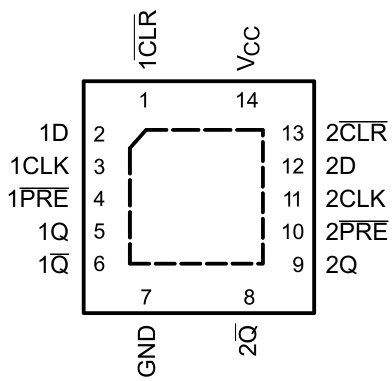
| Changes from Revision L (April 2005) to Revision M | Page |
|---|---|
| • Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Removed Ordering Information table. | 1 |

# 5 Pin Configuration and Functions

**D, DGV, NS, or PW Package**
**14-PIN SOIC, SOP, SSOP, or TSSOP**
**Top View**




**RGY Package**
**14-PIN VQFN**
**Top View**




## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | 1$\overline{\text{CLR}}$ | I | 1 clear |
| 2 | 1D | I | 1D input |
| 3 | 1CLK | I | 1 clock |
| 4 | 1$\overline{\text{PRE}}$ | I | 1 preset |
| 5 | 1Q | O | 1Q output |
| 6 | 1$\overline{\text{Q}}$ | O | 1$\overline{\text{Q}}$ output |
| 7 | GND | – | GND |
| 8 | 2$\overline{\text{Q}}$ | O | 2$\overline{\text{Q}}$ output |
| 9 | 2Q | O | 2Q output |
| 10 | 2$\overline{\text{PRE}}$ | I | 2 preset |
| 11 | 2CLK | I | 2 clock |
| 12 | 2D | I | 2D input |
| 13 | 2$\overline{\text{CLR}}$ | I | 2 clear |
| 14 | Vcc | – | Supply voltage input |

# 6 Specifications

## 6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $V_I$ | Input voltage[2] | | –0.5 | 7 | V |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state[2] | | –0.5 | 7 | V |
| $V_O$ | Output voltage[2][3] | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $\theta_{JA}$ | Package thermal impedance | D package[4] | | 86 | °C/W |
| | | DB package[4] | | 96 | |
| | | DGV package[4] | | 127 | |
| | | NS package[4] | | 76 | |
| | | PW package[4] | | 113 | |
| | | RGY package[5] | | 47 | |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | 2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | 500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | SN54LV74A(2) MIN | SN54LV74A(2) MAX | SN74LV74A MIN | SN74LV74A MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ × 0.7 | | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ × 0.7 | | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ × 0.7 | | $V_{CC}$ × 0.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC}$ × 0.3 | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC}$ × 0.3 | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC}$ × 0.3 | | $V_{CC}$ × 0.3 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | –2 | | –2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | –6 | | –6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 6 | | 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 12 | | 12 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) Product Preview

## 6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | SN54LV74A(1) MIN | SN54LV74A(1) TYP | SN54LV74A(1) MAX | SN74LV74A –40°C to 85°C MIN | SN74LV74A –40°C to 85°C TYP | SN74LV74A –40°C to 85°C MAX | SN74LV74A –40°C to 125°C MIN | SN74LV74A –40°C to 125°C TYP | SN74LV74A –40°C to 125°C MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $I_{OH}$ = –50 µA | 2 V to 5.5 V | $V_{CC}$–0.1 | | | $V_{CC}$–0.1 | | | $V_{CC}$–0.1 | | | V |
| | $I_{OH}$ = –2 mA | 2.3 V | 2 | | | 2 | | | 2 | | | |
| | $I_{OH}$ = –6 mA | 3 V | 2.48 | | | 2.48 | | | 2.48 | | | |
| | $I_{OH}$ = –12 mA | 4.5 V | 3.8 | | | 3.8 | | | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 2 V to 5.5 V | | | 0.1 | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | | | 0.4 | | | 0.4 | |
| | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | | | 0.44 | | | 0.44 | |
| | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | | | 0.55 | | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±1 | | | ±1 | | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | | | 20 | | | 20 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | 0 | | | 5 | | | 5 | | | 5 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 2 | | | 2 | | | 2 | | pF |
| | | 5 V | | 2 | | | 2 | | | 2 | | |

(1) Product Preview

## 6.5 Switching Characteristics: $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54LV74A[1] | | SN74LV74A –40°C to 85°C | | SN74LV74A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 50[2] | 100[2] | | 40[2] | | 40 | | 40 | | MHz |
| | | | $C_L$ = 50 pF | 30 | 70 | | 25 | | 25 | | 25 | | |
| $t_{pd}$ | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ | $C_L$ = 15 pF | | 9.8[2] | 14.8[2] | 1[2] | 17[2] | 1 | 17 | 1 | 18 | ns |
| | CLK | | | | 11.1[2] | 16.4[2] | 1[2] | 19[2] | 1 | 19 | 1 | 20 | |
| $t_{pd}$ | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ | $C_L$ = 50 pF | | 13 | 17.4 | 1 | 20 | 1 | 20 | 1 | 21 | ns |
| | CLK | | | | 14.2 | 20 | 1 | 23 | 1 | 23 | 1 | 24 | |

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.6 Switching Characteristics: $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54LV74A[1] | | SN74LV74A –40°C to 85°C | | SN74LV74A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 80[2] | 140[2] | | 70[2] | | 70 | | 70 | | MHz |
| | | | $C_L$ = 50 pF | 50 | 90 | | 45 | | 45 | | 45 | | |
| $t_{pd}$ | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ | $C_L$ = 15 pF | | 6.9[2] | 12.3[2] | 1[2] | 14.5[2] | 1 | 14.5 | 1 | 15.5 | ns |
| | CLK | | | | 7.9[2] | 11.9[2] | 1[2] | 14[2] | 1 | 14 | 1 | 15 | |
| $t_{pd}$ | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ | $C_L$ = 50 pF | | 9.2 | 15.8 | 1 | 18 | 1 | 18 | 1 | 19 | ns |
| | CLK | | | | 10.2 | 15.4 | 1 | 17.5 | 1 | 17.5 | 1 | 18.5 | |

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.7 Switching Characteristics: $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54LV74A[1] | | SN74LV74A –40°C to 85°C | | SN74LV74A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 130[2] | 180[2] | | 110[2] | | 110 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 90 | 140 | | 75 | | 75 | | 75 | | |
| $t_{pd}$ | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ | $C_L$ = 15 pF | | 5[2] | 7.7[2] | 1[2] | 9[2] | 1 | 9 | 1 | 10 | ns |
| | CLK | | | | 5.6[2] | 7.3[2] | 1[2] | 8.5[2] | 1 | 8.5 | 1 | 9.5 | |
| $t_{pd}$ | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ | $C_L$ = 50 pF | | 6.6 | 9.7 | 1 | 11 | 1 | 11 | 1 | 12 | ns |
| | CLK | | | | 7.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | 1 | 11.5 | |

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.8 Timing Requirements: $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 3)

| | | | $T_A$ = 25°C | | SN54LV74A[1] | | SN74LV74A –40°C to 85°C | | SN74LV74A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low | 8 | | 9 | | 9 | | 9 | | ns |
| | | CLK | 8 | | 9 | | 9 | | 9 | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 8 | | 9 | | 9 | | 9 | | ns |
| | | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive | 7 | | 7 | | 7 | | 7 | | |
| $t_h$ | Hold time, data after CLK↑ | | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |

(1) Product Preview

## 6.9 Timing Requirements: $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)

| | | | $T_A$ = 25°C | | SN54LV74A (1) | | SN74LV74A –40°C to 85°C | | SN74LV74A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 6 | | 7 | | 7 | | 7 | | ns |
| | | CLK | 6 | | 7 | | 7 | | 7 | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 6 | | 7 | | 7 | | 7 | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | 5 | | 5 | | 5 | | 5 | | |
| $t_h$ | Hold time, data after CLK↑ | | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |

(1) Product Preview

## 6.10 Timing Requirements: $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

| | | | $T_A$ = 25°C | | SN54LV74A (1) | | SN74LV74A –40°C to 85°C | | SN74LV74A –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 5 | | 5 | | 5 | | 5 | | ns |
| | | CLK | 5 | | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 5 | | 5 | | 5 | | 5 | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | 3 | | 3 | | 3 | | 3 | | |
| $t_h$ | Hold time, data after CLK↑ | | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |

(1) Product Preview

## 6.11 Noise Characteristics (1)

$V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER | | SN74LV74A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.1 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | 0 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 3.2 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

(1) Characteristics are for surface-mount packages only.

## 6.12 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF | f = 10 MHz | 3.3 V | 21 | pF |
| | | | | 5 V | 23 | |

## 6.13 Typical Characteristics

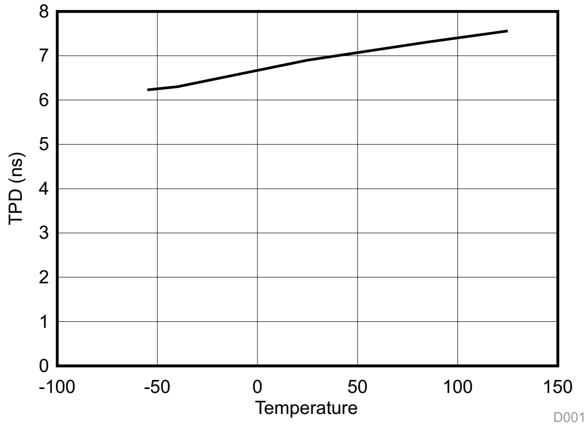



**Figure 1. TPD vs. Temperature at 3.3 V**

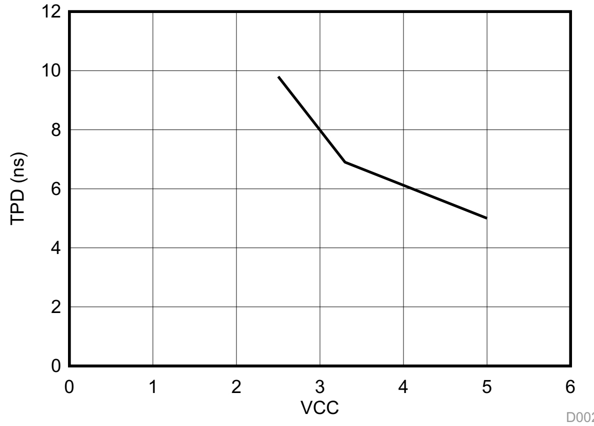
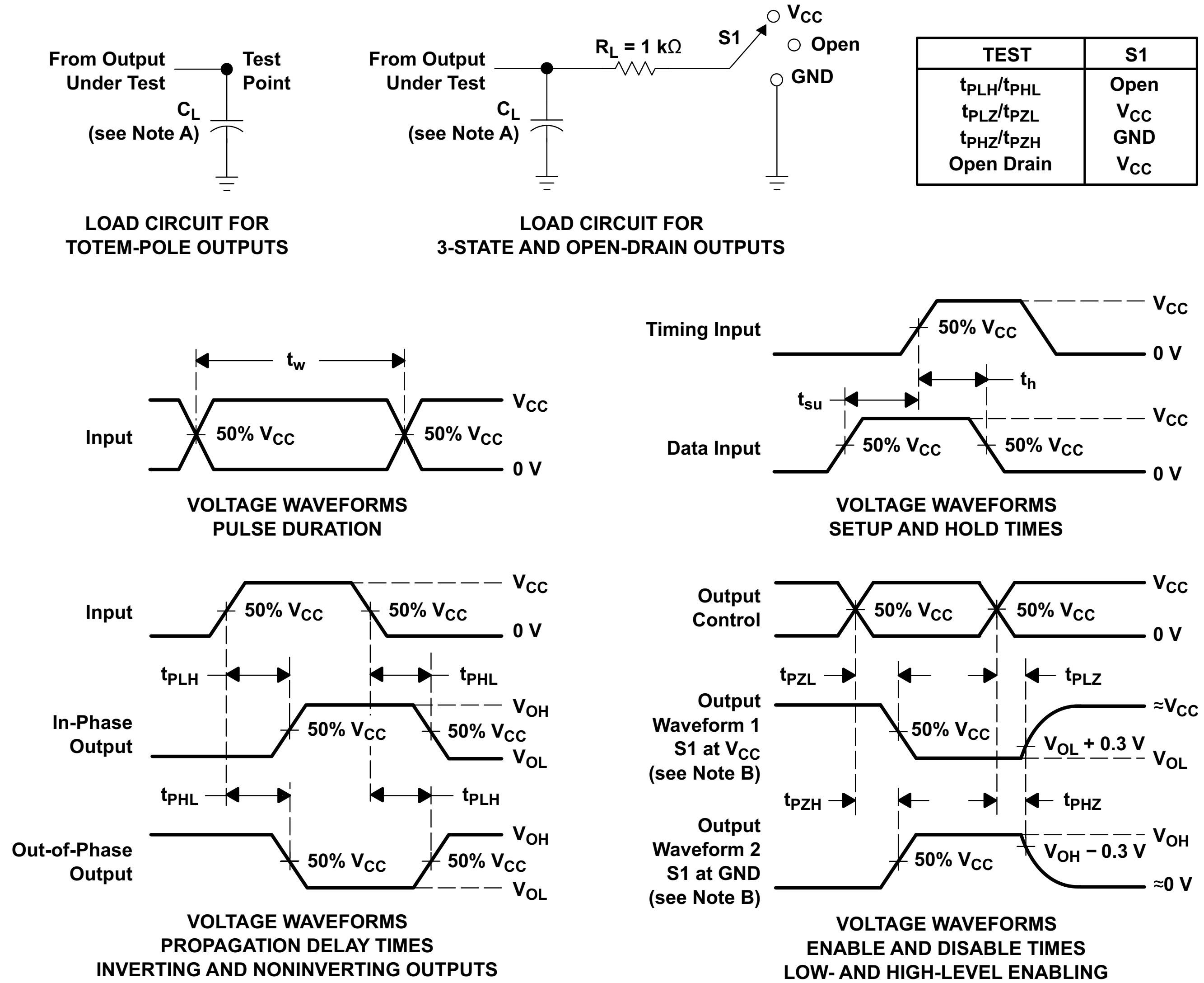



**Figure 2. TPD vs. VCC at 25°C**

# 7 Parameter Measurement Information




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r \le 3$ ns, $t_f \le 3$ ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

These dual positive-edge-triggered D-type flip-flops are designed for 2-V to 5.5-V $V_{CC}$ operation.

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs. The state of the output upon power-up is not known until the first valid clock edge has occurred while $V_{CC}$ is within *Recommended Operating Conditions*.

These devices are fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

## 8.2 Functional Block Diagram

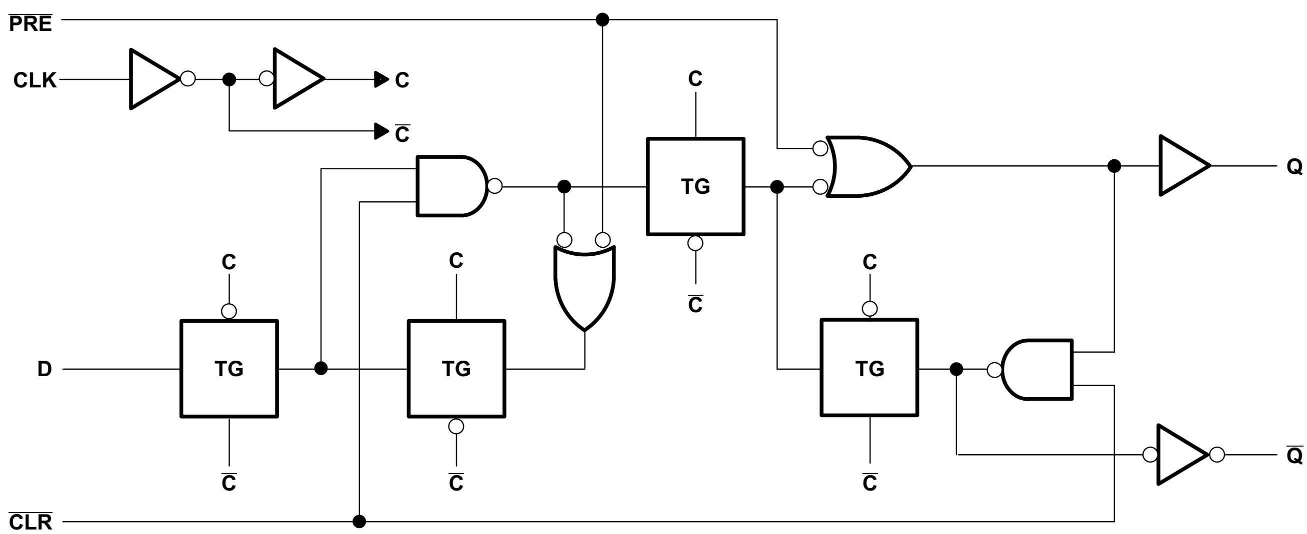



**Figure 4. Logic Diagram, Each Flip-Flop (Positive Logic)**

## 8.3 Feature Description

The device's wide operating range allows it to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.

## 8.4 Device Functional Modes

**Table 1. Function Table**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q | Q |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H[1] | H[1] |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

(1) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LV74A is a Low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid $V_{CC}$ making it Ideal for down translation.

## 9.2 Typical Application

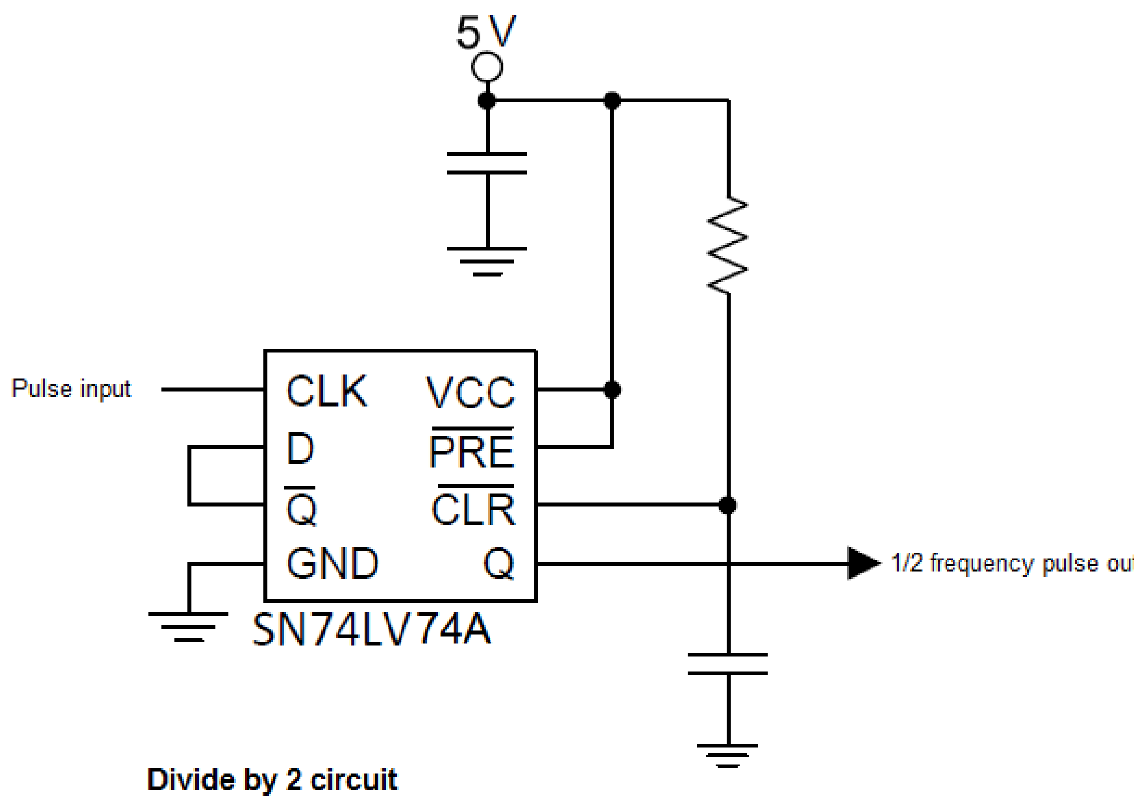



**Figure 5. Typical Application Schematic**

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Specified High and low levels. See ($V_{IH}$ and $V_{IL}$) in *Recommended Operating Conditions*.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$.
- Recommended output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above $V_{CC}$.

### 9.2.3 Application Curves

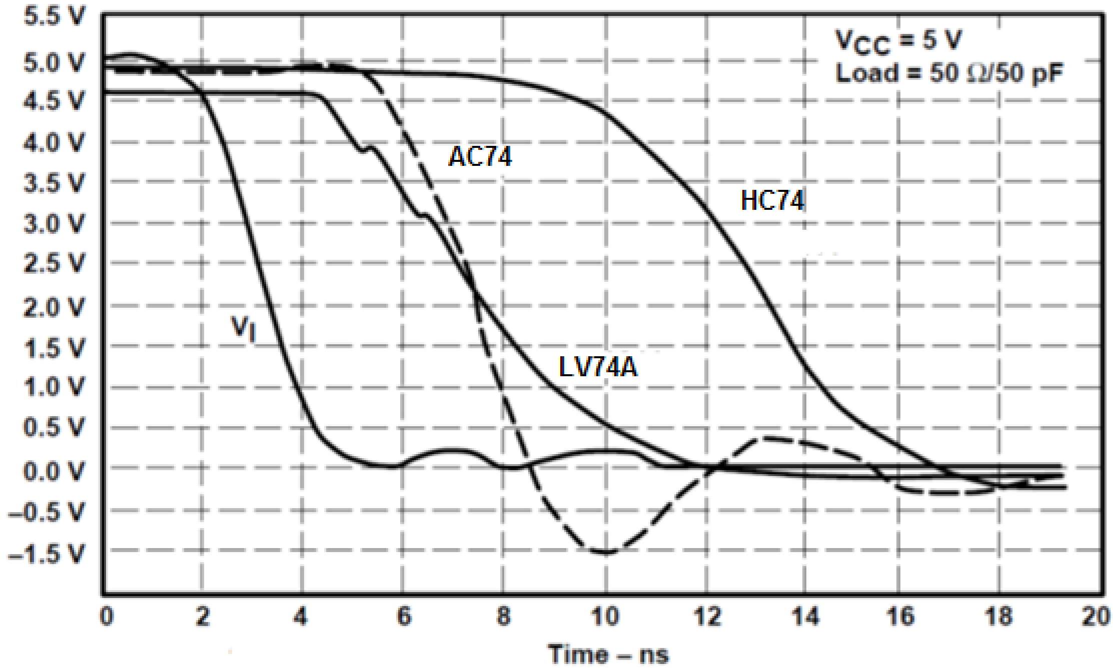



**Figure 6. Switching Characteristics Comparison**

# 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF capacitor and if there are multiple $V_{CC}$ terminals then TI recommends a 0.01-μF or 0.022-μF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

# 11 Layout

## 11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$ whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

## 11.2 Layout Example

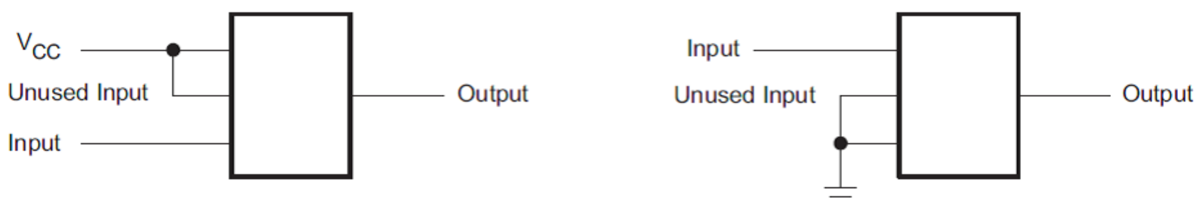



**Figure 7. Layout Recommendation**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

*Implications of Slow or Floating CMOS Inputs*, SCBA004

## 12.2 Trademarks

All trademarks are the property of their respective owners.

## 12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV74AD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV74A | Samples |
| SN74LV74ADBLE | OBSOLETE | SSOP | DB | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74LV74ADBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV74A | Samples |
| SN74LV74ADG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV74A | Samples |
| SN74LV74ADGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV74A | Samples |
| SN74LV74ADR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV74A | Samples |
| SN74LV74ADRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV74A | Samples |
| SN74LV74ANSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV74A | Samples |
| SN74LV74APW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV74A | Samples |
| SN74LV74APWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV74A | Samples |
| SN74LV74APWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74LV74APWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 125 | LV74A | Samples |
| SN74LV74APWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV74A | Samples |
| SN74LV74APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV74A | Samples |
| SN74LV74APWT | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV74A | Samples |
| SN74LV74ARGYR | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV74A | Samples |
| SN74LV74ARGYRG4 | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV74A | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

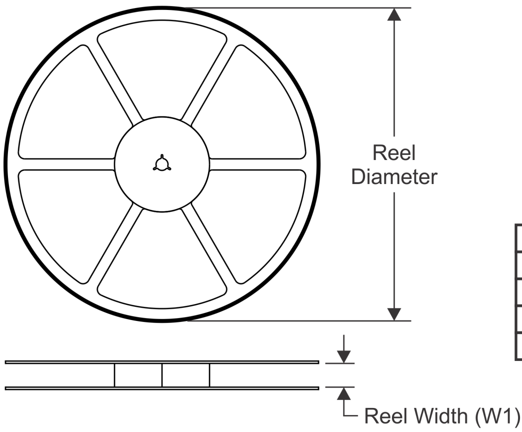
**OTHER QUALIFIED VERSIONS OF SN74LV74A :**

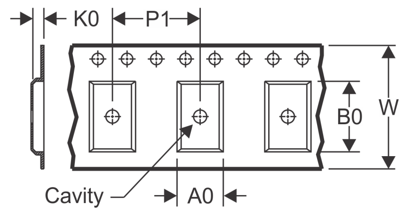
- Automotive: SN74LV74A-Q1
- Enhanced Product: SN74LV74A-EP

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

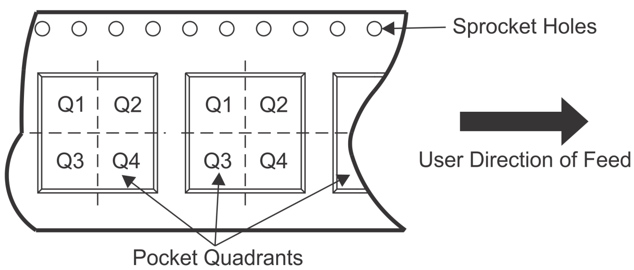
## TAPE AND REEL INFORMATION




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

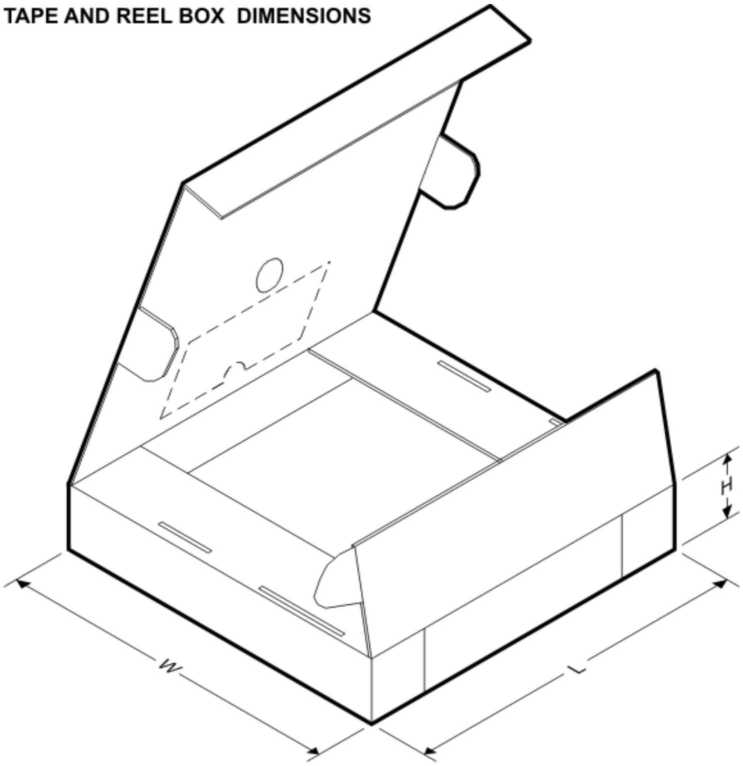
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV74ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV74ADGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV74ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV74APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV74APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV74APWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV74APWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV74ARGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

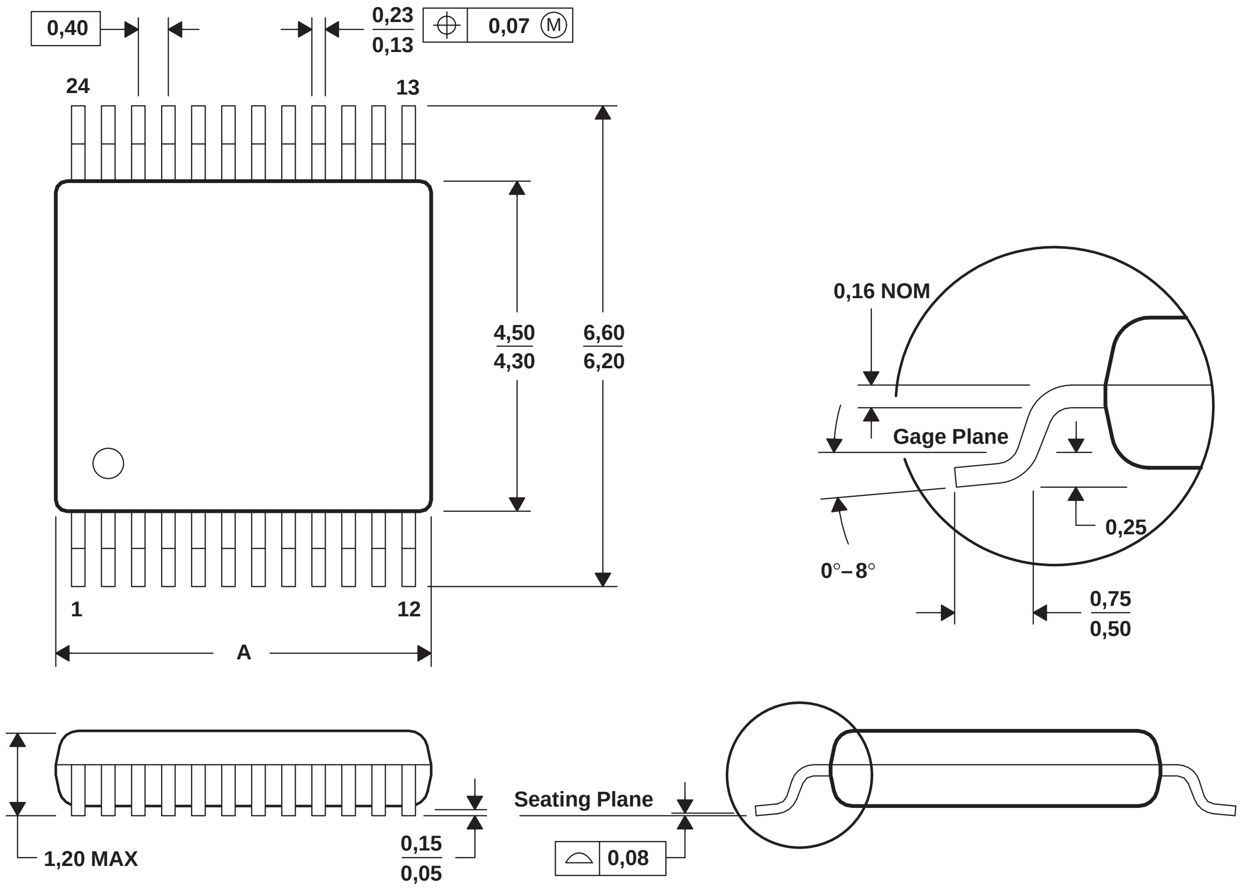



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV74ADBR | SSOP | DB | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV74ADGVR | TVSOP | DGV | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV74ADR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74LV74APWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV74APWR | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV74APWRG4 | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV74APWT | TSSOP | PW | 14 | 250 | 367.0 | 367.0 | 35.0 |
| SN74LV74ARGYR | VQFN | RGY | 14 | 3000 | 367.0 | 367.0 | 35.0 |

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

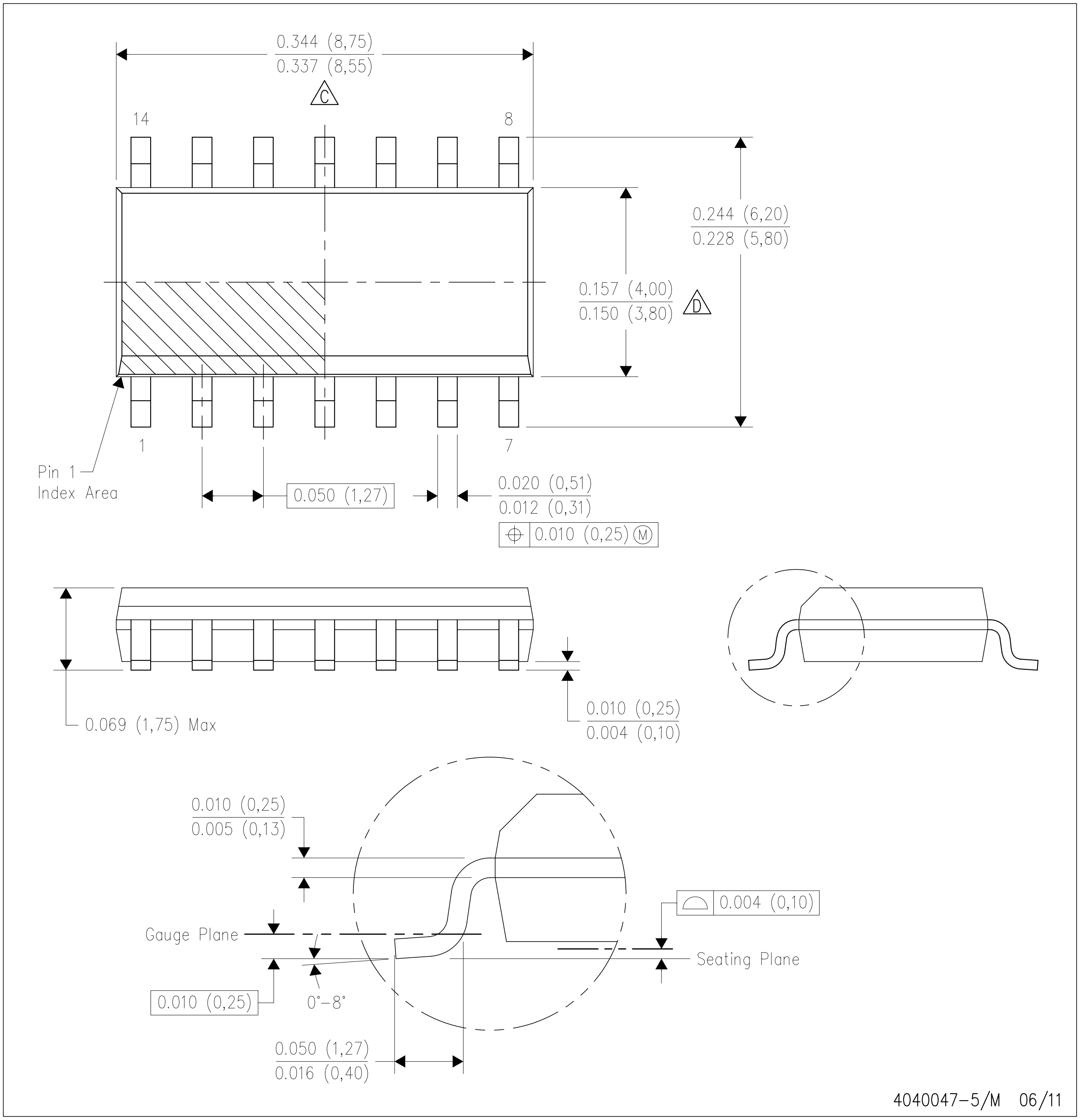



| PINS ** / DIM | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| **A MAX** | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| **A MIN** | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

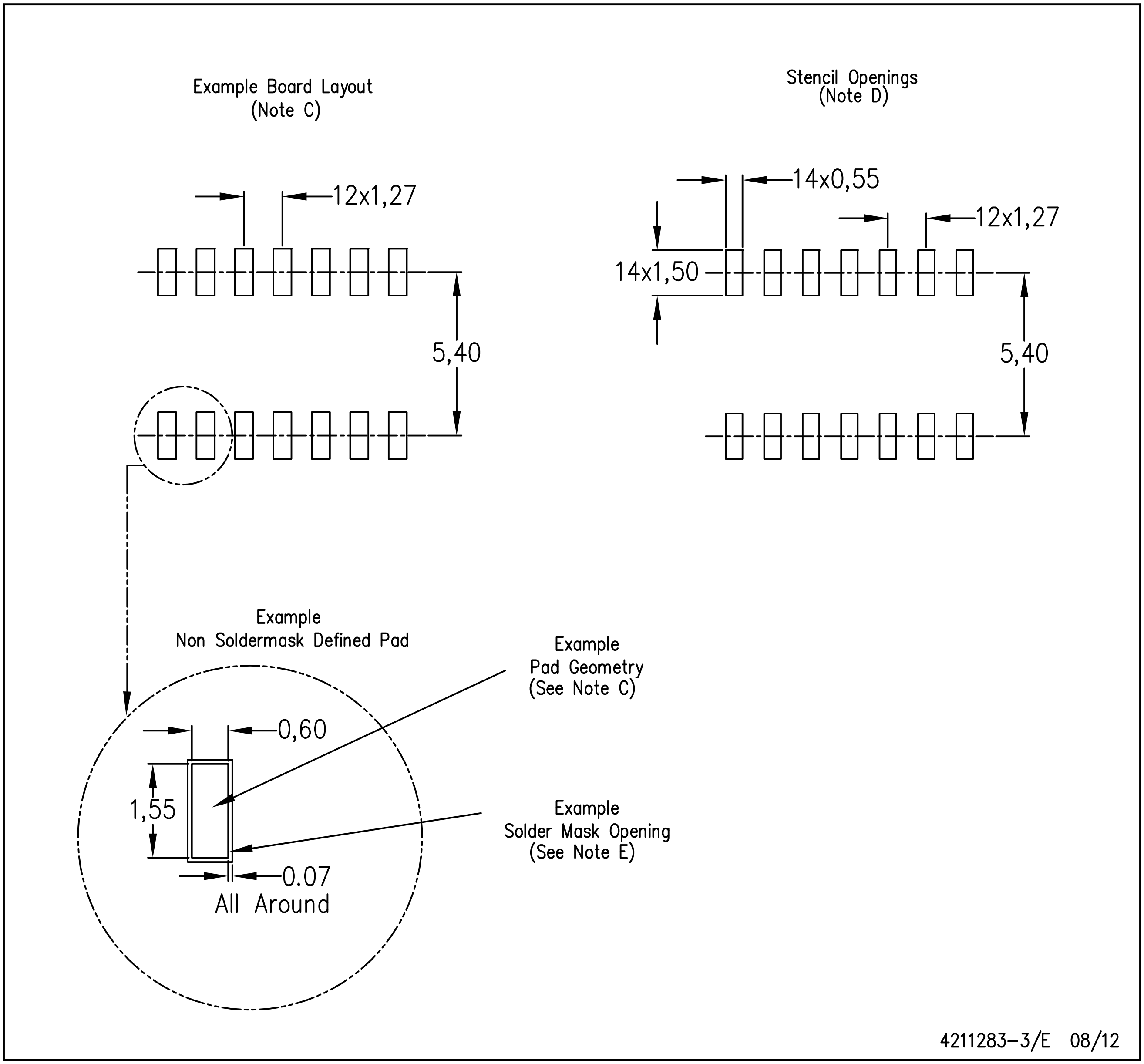
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



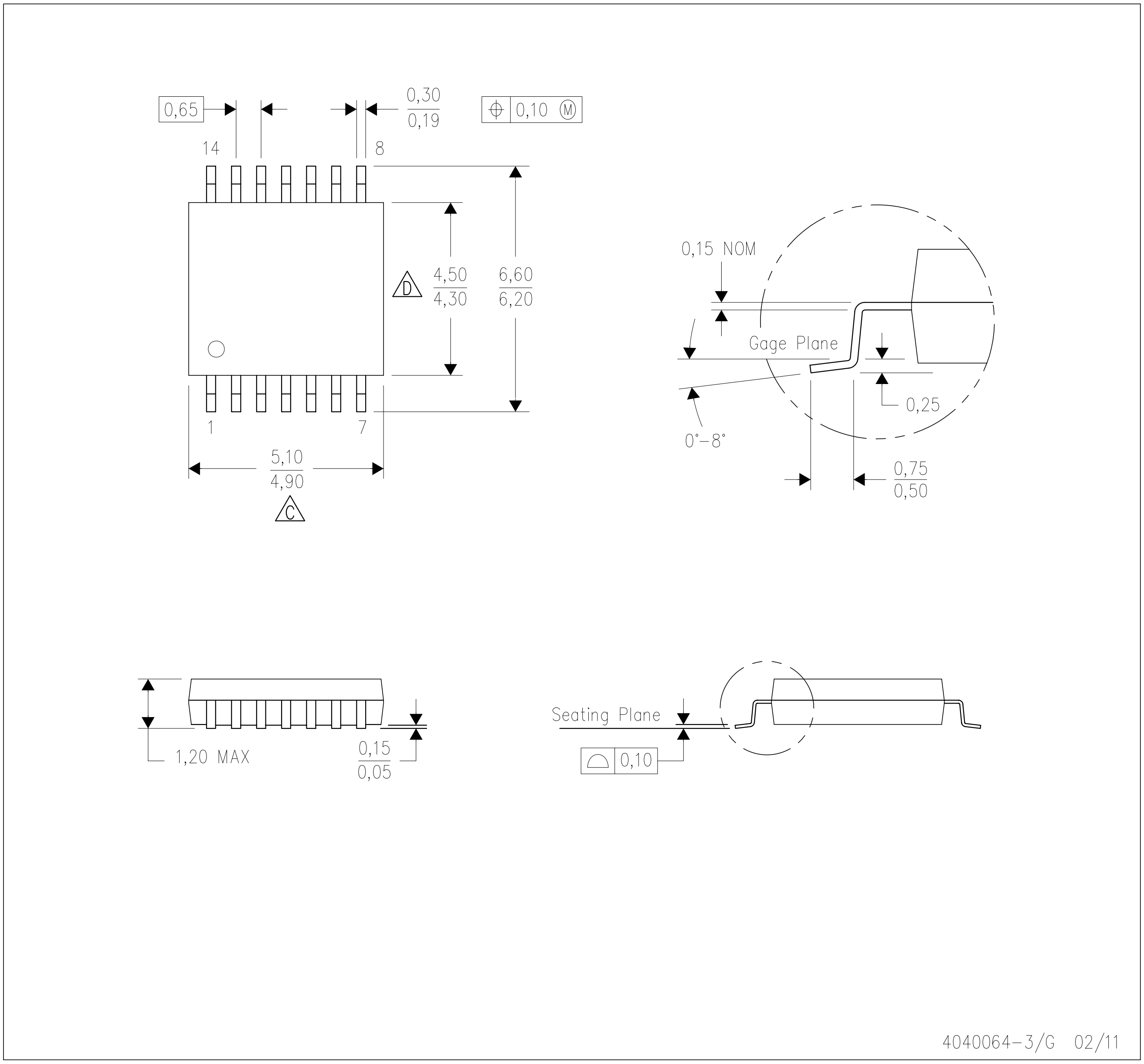

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



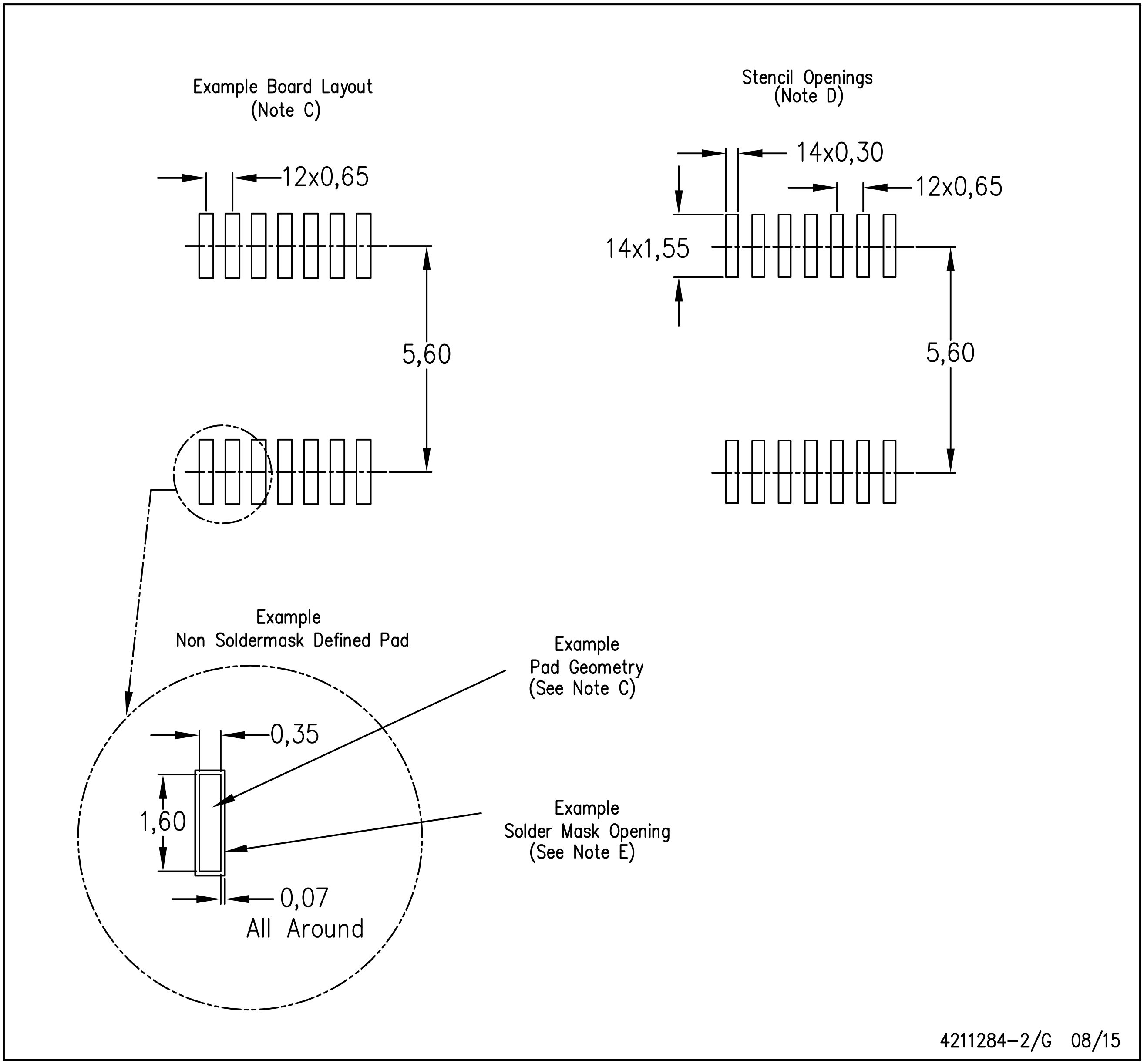

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

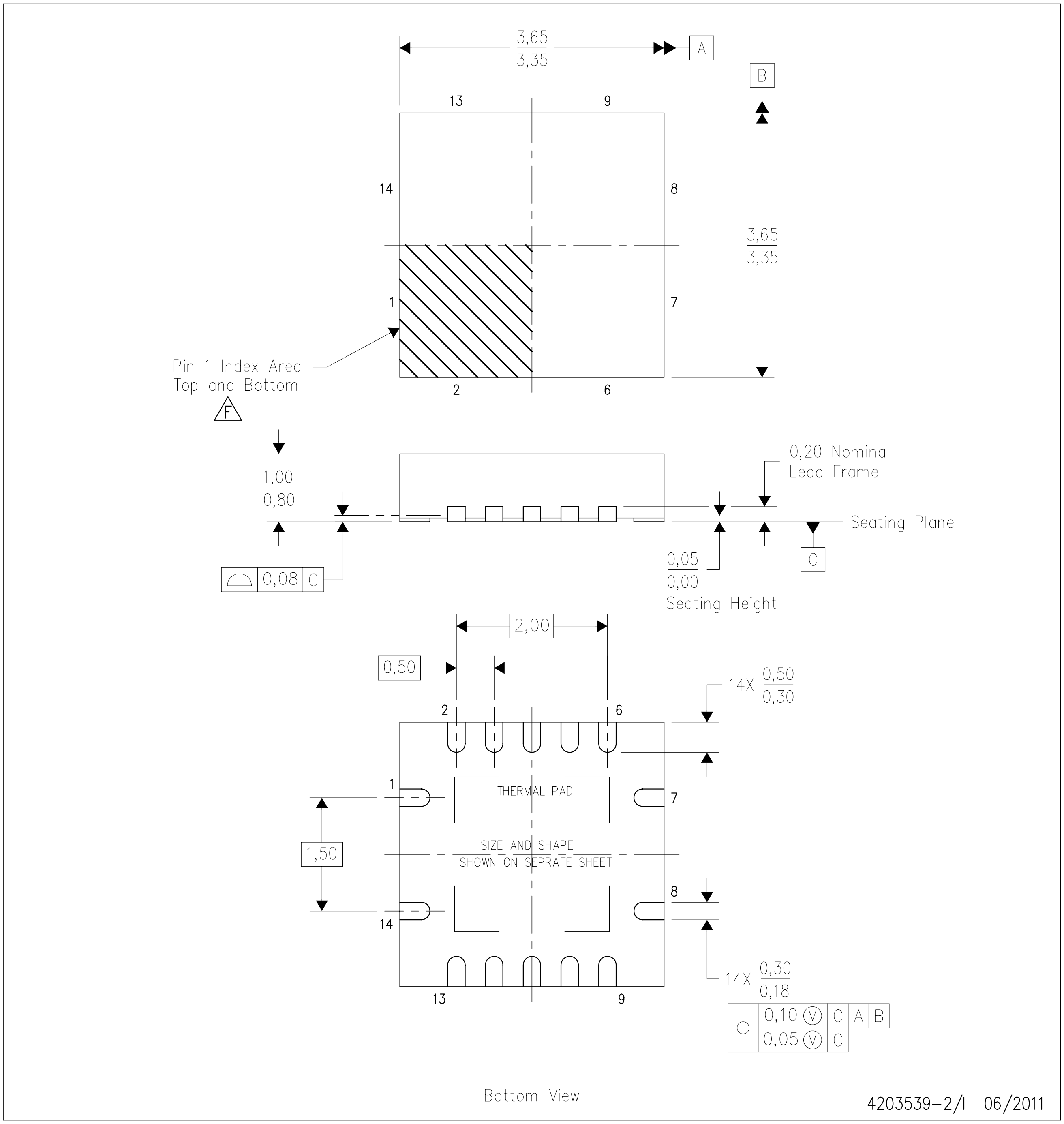
PW (R-PDSO-G14) PLASTIC SMALL OUTLINE




NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO-241 variation BA.

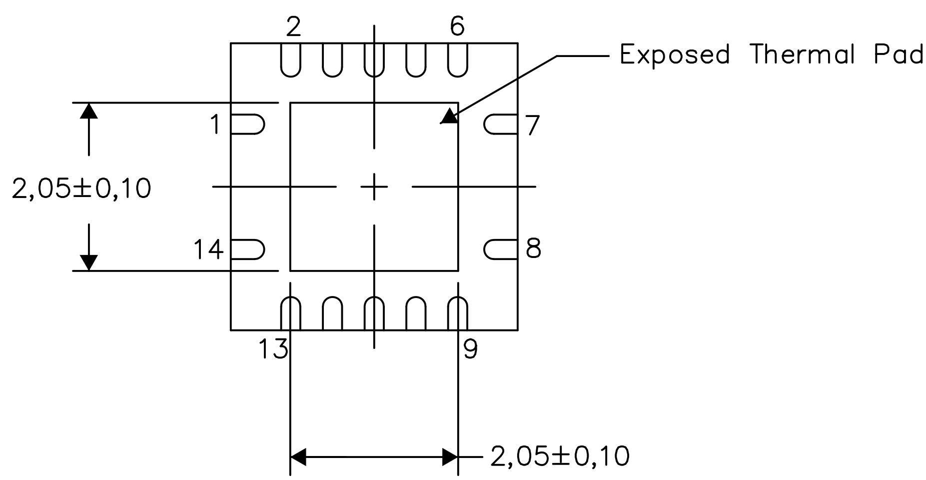
RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



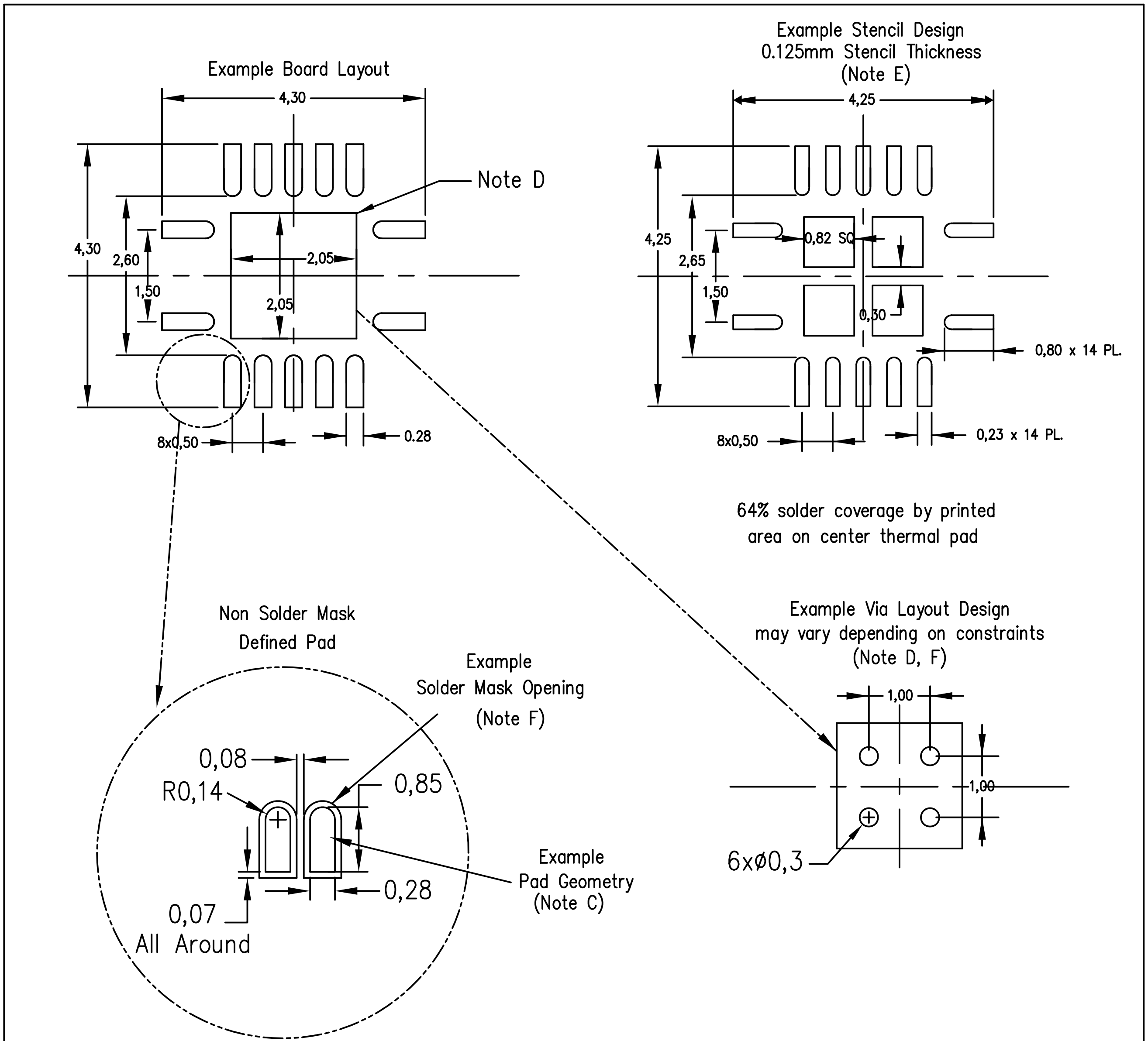

Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD

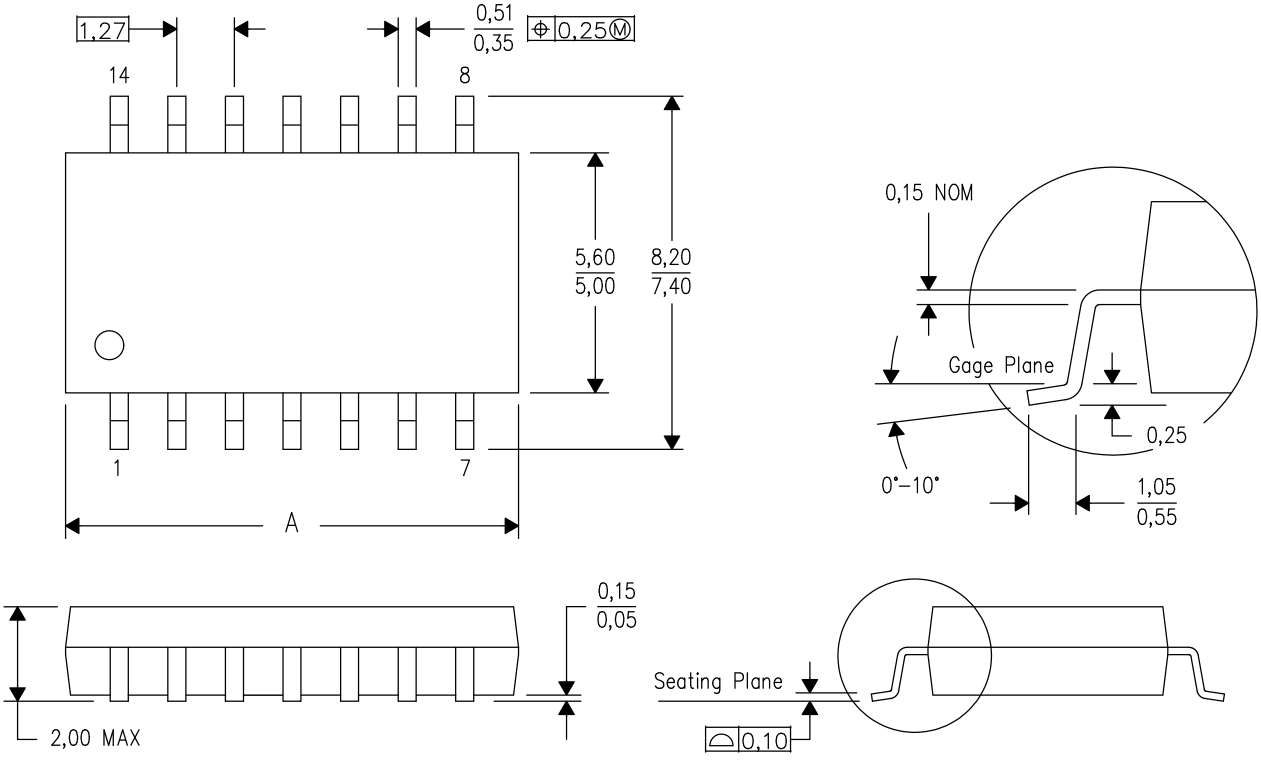



4208122-2/P 03/14

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



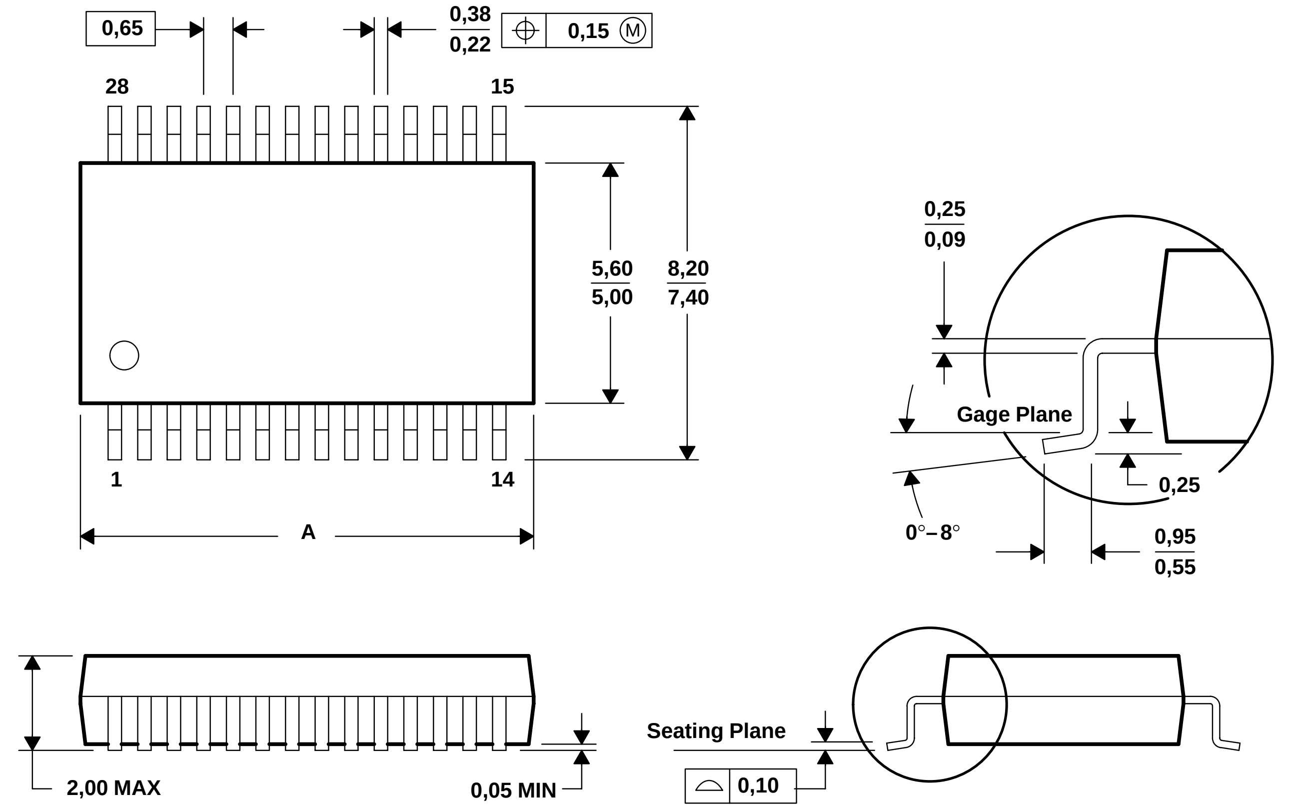

| PINS ** / DIM | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| PINS ** / DIM | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150