LM2904

Low power dual operational amplifier

Features

- Internally frequency compensated
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1.1MHz (temperature compensated)
- Very low supply current/op (500µA) essentially independent of supply voltage
- Low input bias current: 20nA (temperature compensated)
- Low input offset current: 2nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to (V_{CC} - 1.5V)

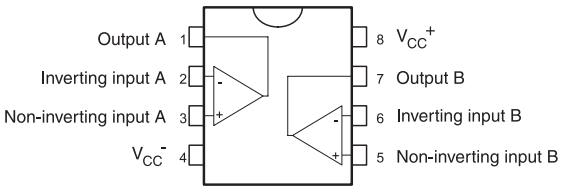
N
DIP8
(Plastic Package)

D
SO-8
(Plastic Micropackage)

P
TSSOP8
(Thin Shrink Small Outline Package)

S
Mini SO-8
(Mini SO Package)

Pin connections (top view)



Description

This circuit consists of two independent, high gain, internally frequency compensated which were designed specifically for automotive and industrial control system. It operates from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with off the standard +5V which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

Contents

1 Device summary table

Part number	Temperature range	Package	Packing	Marking
LM2904N	-40°C to +125°C	DIP8	Tube	LM2904N
LM2904D/DT		SO-8	Tube or Tape & Reel	2904
LM2904PT		TSSOP8 (Thin Shrink Outline Package)	Tape & Reel	
LM2904ST		mini SO-8	Tape & Reel	K403
LM2904YD/YDT		SO-8 (automotive grade level)	Tube or Tape & Reel	2904Y
LM2904YPT		TSSOP8 (automotive grade level)	Tape & Reel	
LM2904YST		minI SO-8 (automotive grade level)	Tape & Reel	k409

2 Absolute maximum ratings

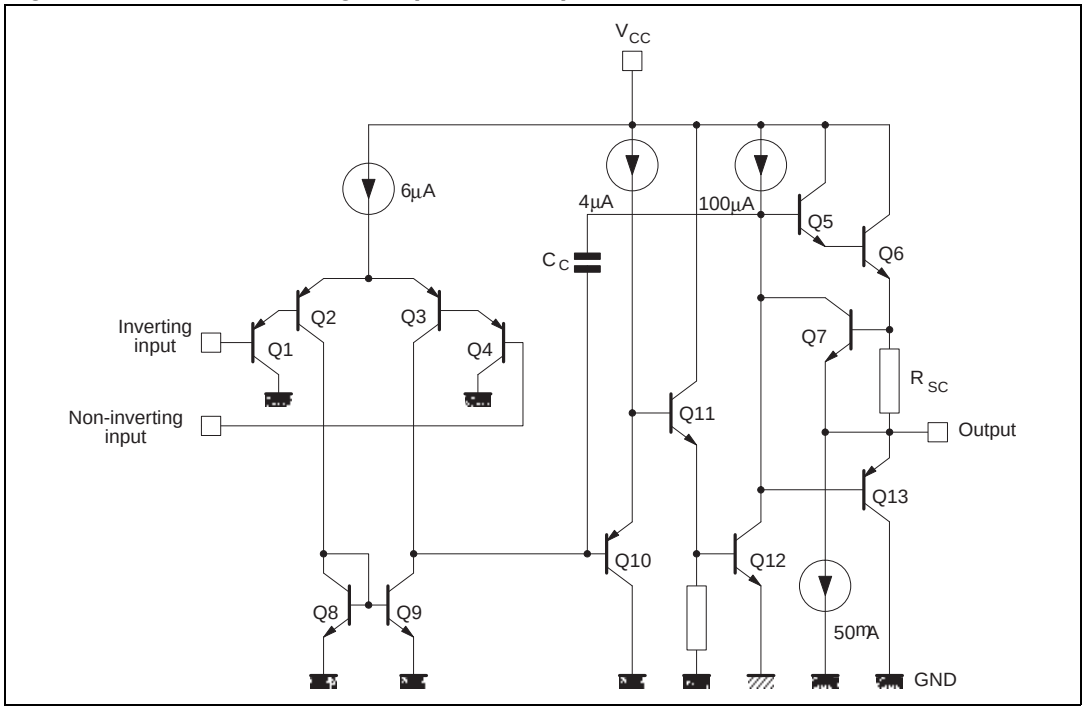
Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	±16 or 32	V
V_{id}	Differential input voltage(2)	±32	V
V_i	Input voltage	-0.3 to 32	V
	Output short-circuit to ground (3)		
p_{tot}	Power dissipation (4)	500	mW
I_{in}	Input current (5)	50	mA
T_{oper}	Operating free-air temperature range	-40 to +125	°C
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient(6) SO-8 TSSOP8 DIP8 MiniSO-8	 125 120 85 190	°C/W
R_{thjc}	Thermal resistance junction to case SO-8 TSSOP8 DIP8 MiniSO-8	 40 37 41 39	°C/W
ESD	HBM: human body model(7)	500	V
	MM: machine model(8)	100	V
	CDM: charged device model	1.5	kV

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. Short-circuits from the output to V_{CC} can cause excessive heating if $Vcc^+ > 15V$. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC}.
   Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
4. Power dissipation must be considered to ensure maximum junction temperature (Tj) is not exceeded.
5. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diodes clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative. This is not destructive and normal output will set up again for input voltage higher than -0.3V.
6. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
7. Human body model, 100pF discharged through a 1.5kΩ resistor into pin of device.
8. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin to pin of device.

3 Typical application schematic

Figure 1. Schematic Diagram (1/2 LM2904)



4 Electrical characteristics

Table 2. V_{CC}^+ = 5V, V_{cc}^- = Ground, V_O = 1.4V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max.}$		2	7 9	mV
I_{io}	Input offset current T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max.}$		2	30 40	nA
I_{ib}	Input bias current (2) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max.}$		20	150 200	nA
A_{vd}	Large signal voltage gain V_{CC}^+ = +15V,R_L=2kΩ, V_o = 1.4V to 11.4V T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max.}$	 50 25	100		V/mV
SVR	Supply voltage rejection ratio (R_S ≤10kΩ) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max.}$	65 65	100		dB
I_{cc}	Supply current, all amp, no load T_{amb} = 25°C, V_{CC} = +5V $T_{min} \le T_{amb} \le T_{max.}$, V_{CC} = +30V		0.7	1.2 2	mA
V_{icm}	Input common mode voltage range (V_{cc}= +30V) (3) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max.}$	0 0		V_{CC}^+ -1.5 V_{CC}^+ -2	V
CMR	Common-mode rejection ratio (R_S = 10kΩ) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max.}$	70 60	85		dB
I_{source}	Output short-circuit current V_{CC} = +15V, V_o = +2V, V_{id} = +1V	20	40	60	mA
I_{sink}	Output sink current V_O = 2V, V_{CC} = +5V V_O = +0.2V, V_{CC} = +15V	10 12	20 50		mA µA
V_{OPP}	Output voltage swing (R_L = 2kΩ T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$	0 0		V_{CC}^+ -1.5 V_{CC}^+ -2	V
V_{OH}	High level output voltage (V_{cc} + 30V) T_{amb} = +25°C, R_L = 2kΩ $T_{min} \le T_{amb} \le T_{max.}$ T_{amb} = +25°C, R_L = 10kΩ $T_{min} \le T_{amb} \le T_{max.}$	26 26 27 27	27 28		V
V_{OL}	Low level output voltage (R_L = 10kΩ) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		5	20 20	mV

Table 2. V_{CC}^+ = 5V, V_{cc}^- = Ground, V_O = 1.4V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SR	Slew rate V_{cc} = 15V, Vi = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, unity gain $T_{min} \leq T_{amb} \leq T_{max}$	0.3 0.2	0.6		V/µs
GBP	Gain bandwidth product f = 100kHz V_{cc} = 30V, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF	0.7	1.1		MHz
THD	Total harmonic distortion f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_o = 2Vpp, C_L = 100pF, V_{cc} = 30V		0.02		%
DV_{io}	Input offset voltage drift		7	30	µV/°C
DI_{io}	Input offset current drift		10	300	pA/°C
V_{O1}/V_{O2}	Channel separation (4) 1kHz ≤ f ≤ 20kHz		120		dB

1. V_O = 1.4V, R_S = 0Ω, 5V < V_{CC}^+ < 30V, 0V < V_{ic} < V_{CC}^+ - 1.5V.
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output, so no loading charge change exists on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^+ –1.5V, but either or both inputs can go to +32V without damage.
4. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Figure 2. Open loop frequency response

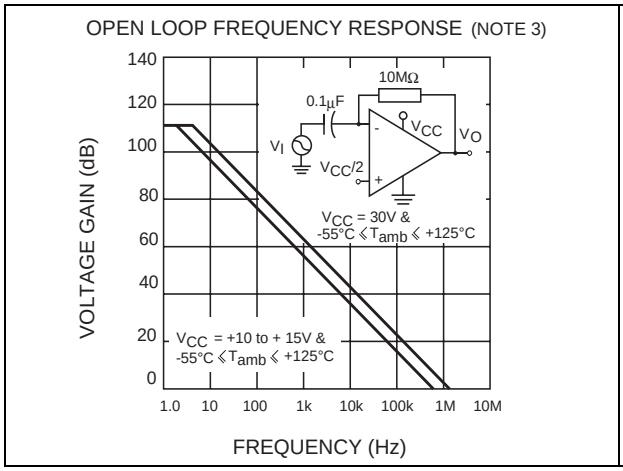


Figure 3. Large signal frequency response

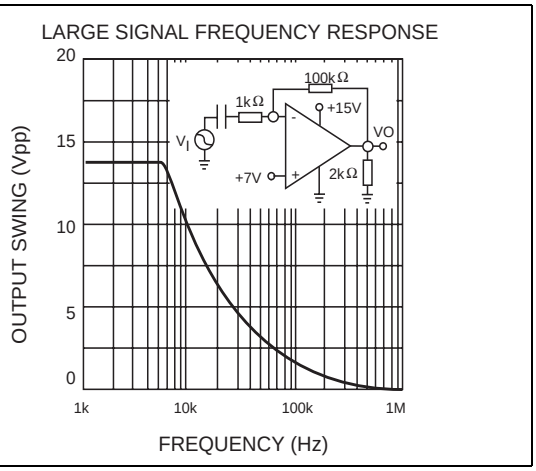


Figure 4. Voltage follower pulse response

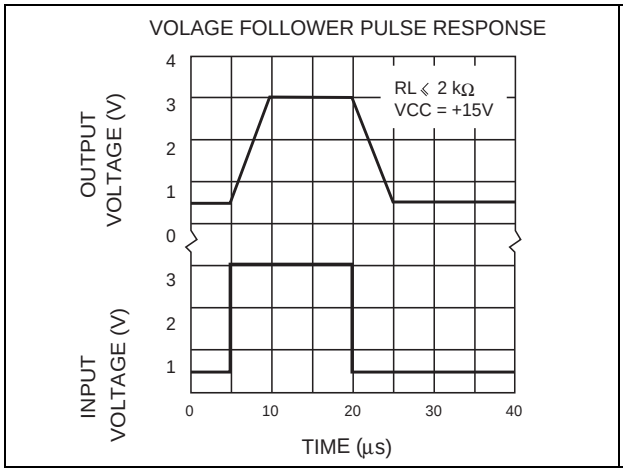


Figure 5. Output characteristics

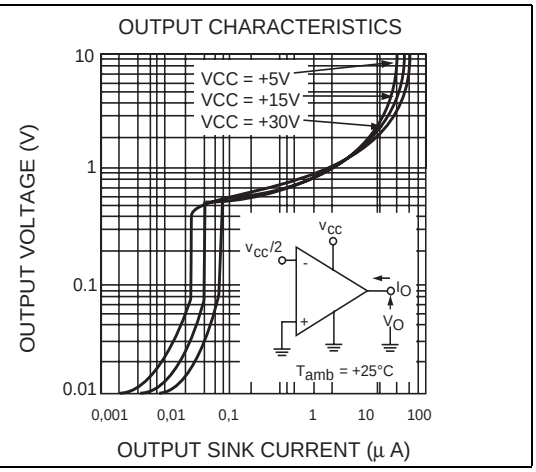


Figure 6. Voltage follower pulse response

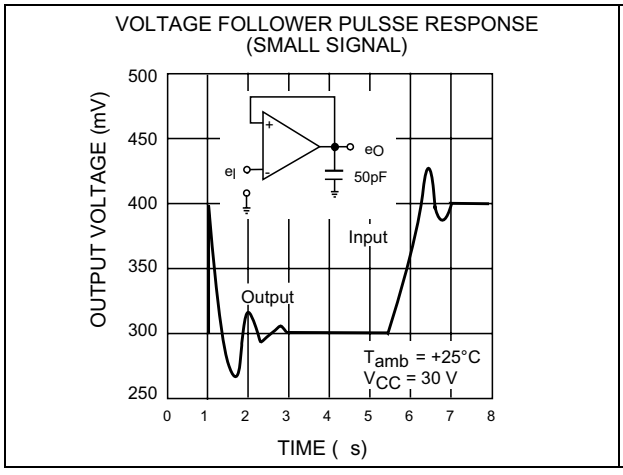


Figure 7. Output characteristics

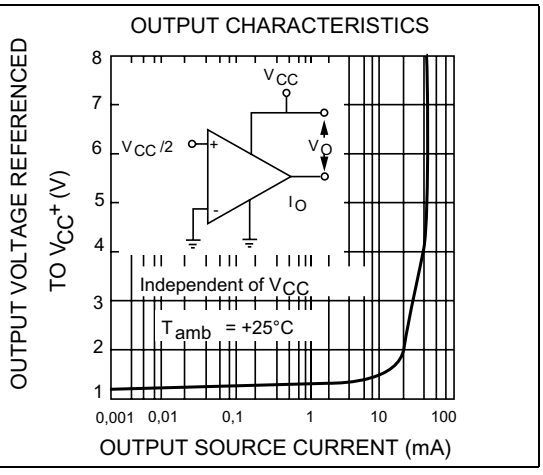


Figure 8. Input current

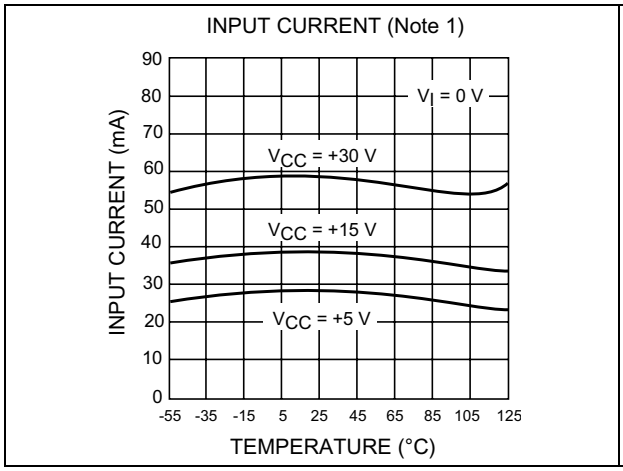


Figure 9. Current limiting

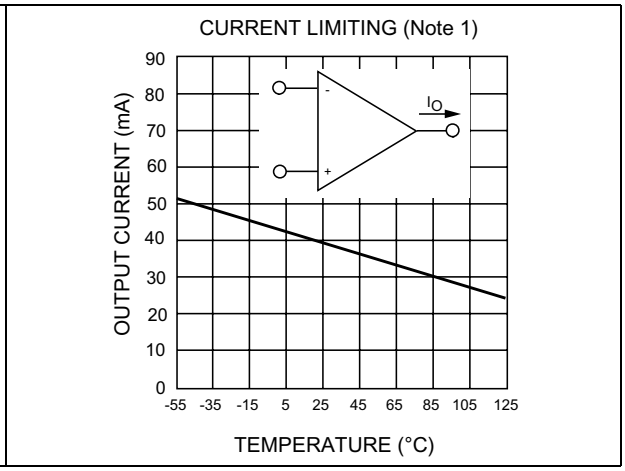


Figure 10. Input voltage range

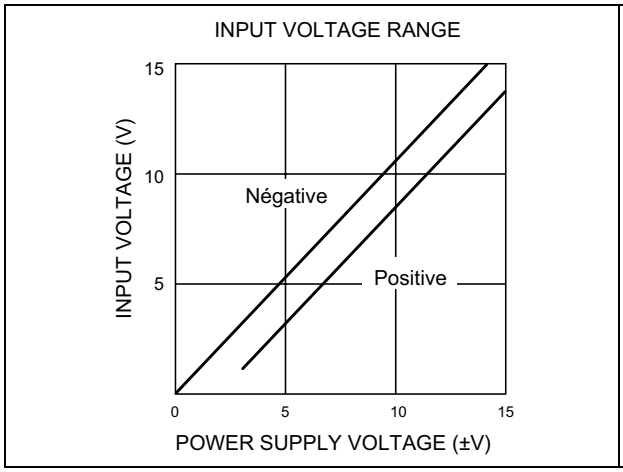


Figure 11. Supply current

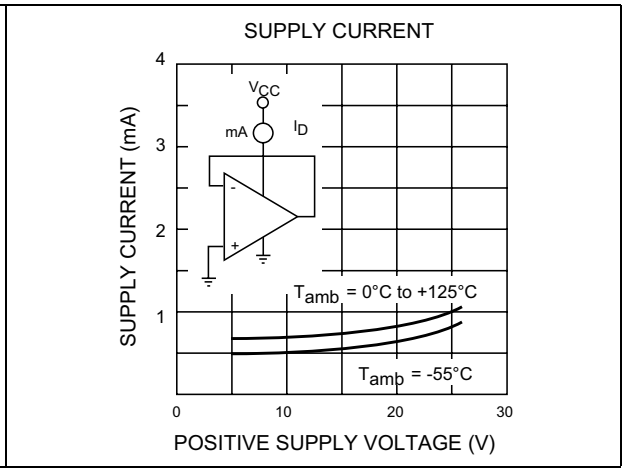


Figure 12. Positive supply voltage

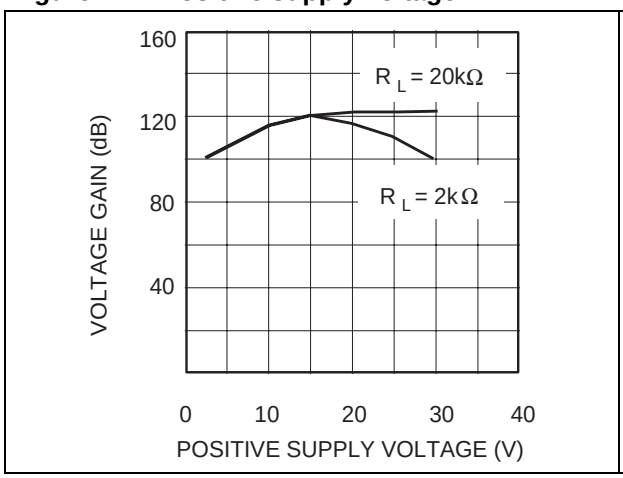


Figure 13. Positive supply voltage

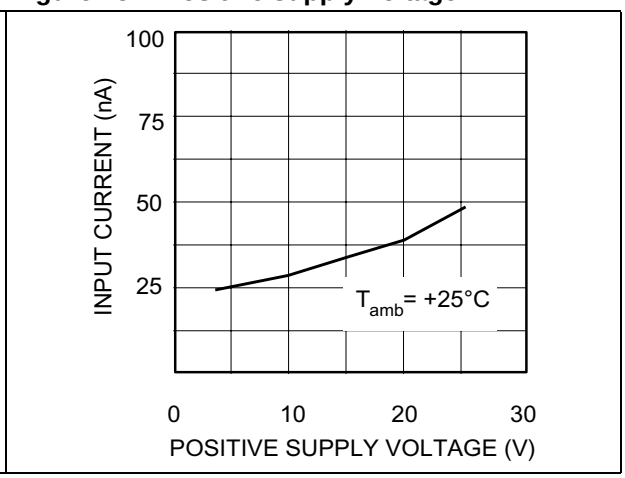


Figure 14. Positive supply voltage

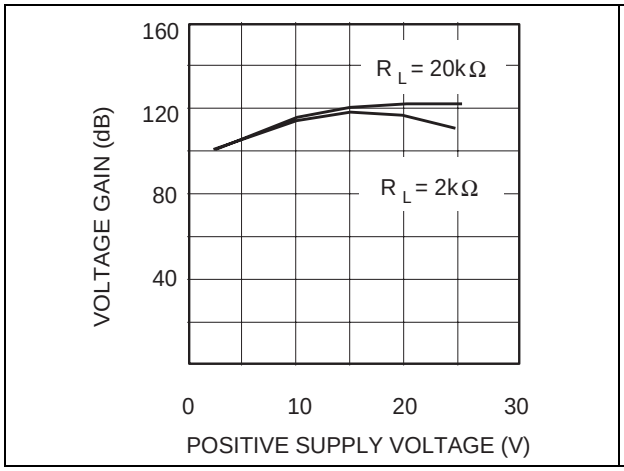


Figure 15. Gain bandwidth product

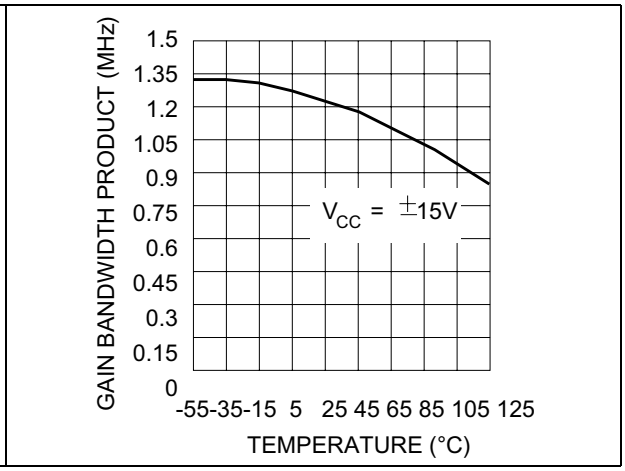


Figure 16. Power supply rejection ratio

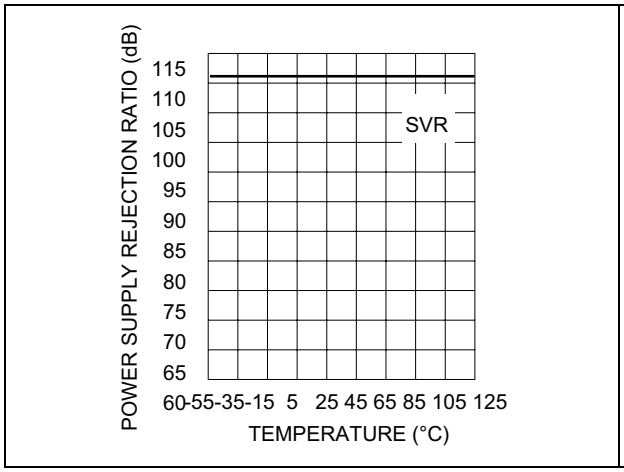
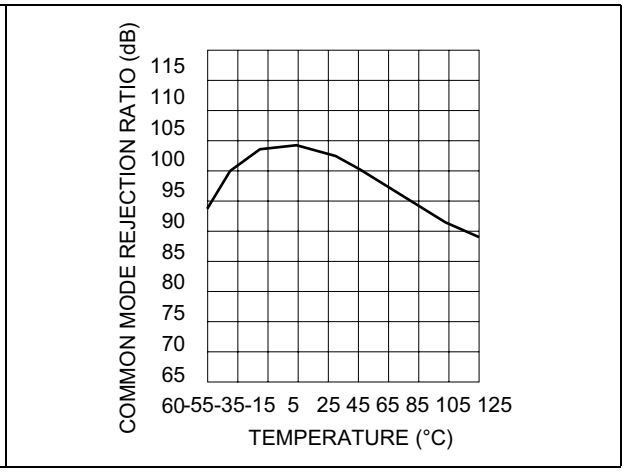


Figure 17. Common mode rejection ratio



Typical single - supply applications

Figure 18. AC coupled inverting amplifier

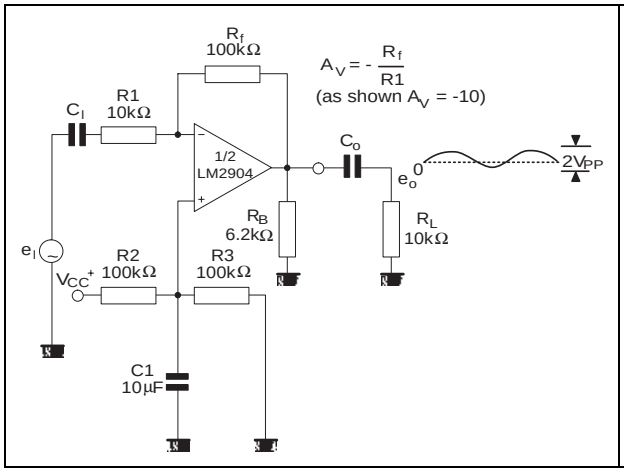


Figure 19. AC coupled non-inverting amplifier

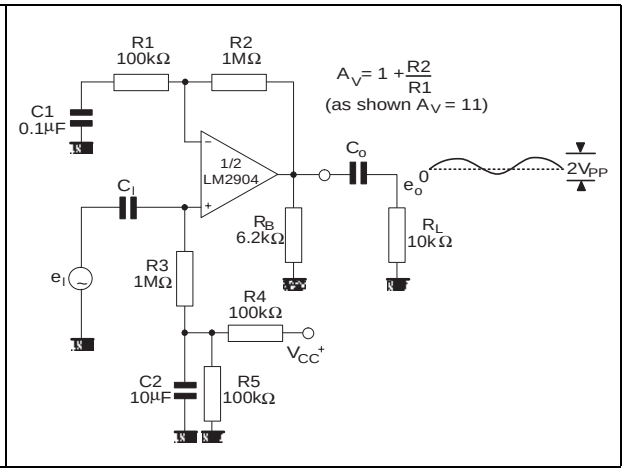


Figure 20. Non-inverting DC gain

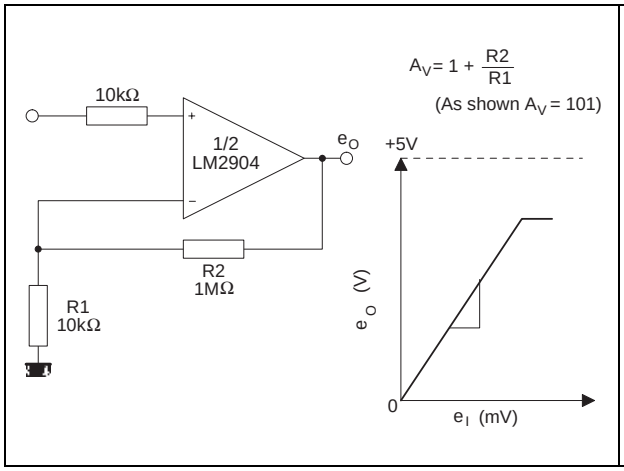


Figure 21. DC summing amplifier

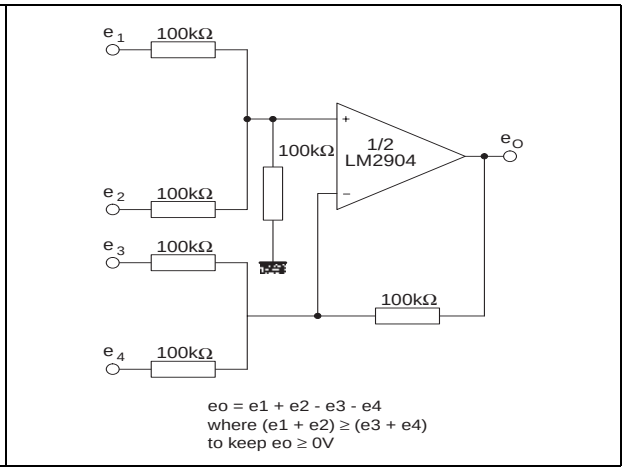


Figure 22. High input Z, DC differential amplifier

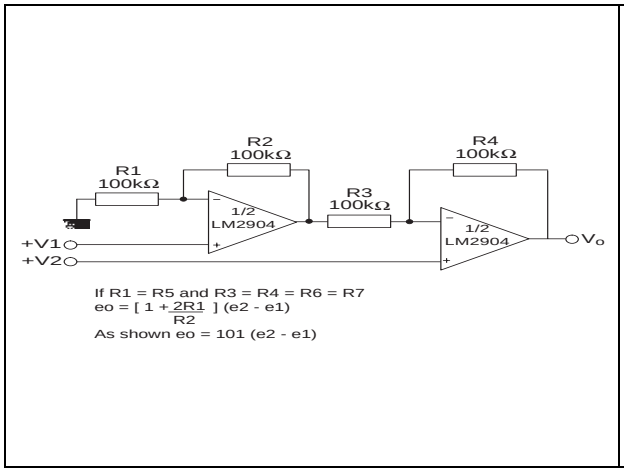


Figure 23. Using symmetrical amplifiers to reduce input current

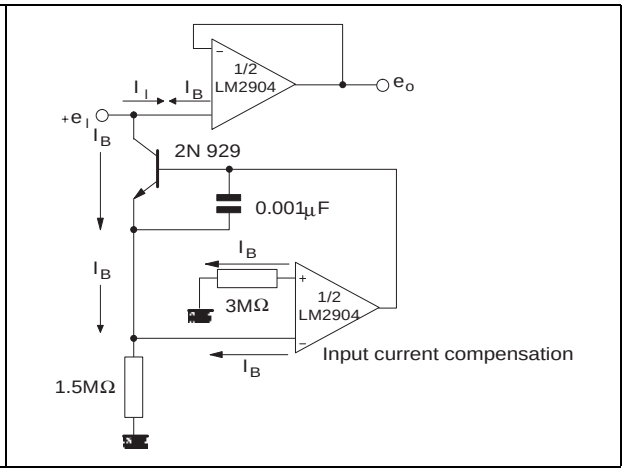


Figure 24. Low drift peak detector

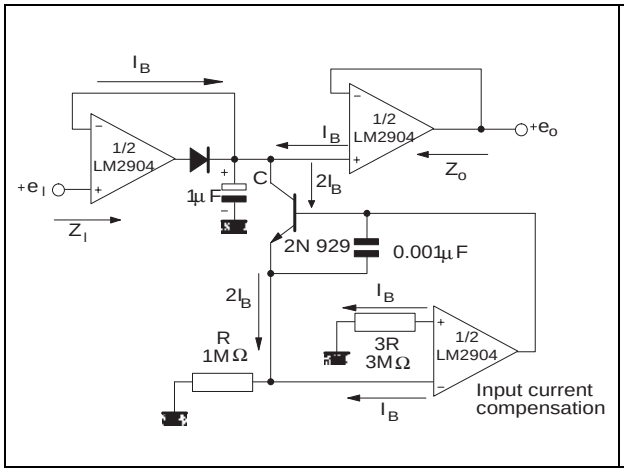
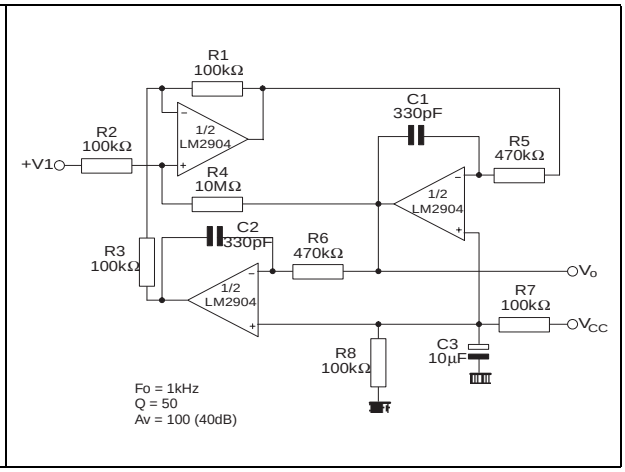


Figure 25. Active bandpass filter



5 Macromodel

5.1 Important note concerning this macromodel

Please consider following remarks before using this macromodel.

- All models are a trade-off between accuracy and complexity (i.e. simulation time).
- Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
- A macromodel emulates the NOMINAL performance of a TYPICAL device within SPECIFIED OPERATING CONDITIONS (i.e. temperature, supply voltage, etc.). Thus the macromodel is often not as exhaustive as the datasheet, its goal is to illustrate the main parameters of the product.

Data issued from macromodels used outside of its specified conditions (Vcc, Temperature, etc.) or even worse: outside of the device operating conditions (Vcc, Vicm, etc.) are not reliable in any way.

5.2 Macromodel code

```
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
.SUBCKT LM2904 1 2 3 4 5
*************************
.MODEL MDTH D IS=1E-8 KF=3.104131E-15 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E+01
RIN 15 16 2.600000E+01
RIS 11 15 2.003862E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-05
CPS 11 15 3.783376E-09
DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 2.000000E+00
FCP 4 5 VOFP 3.400000E+01
FCN 5 4 VOFN 3.400000E+01
FIBP 2 5 VOFN 2.000000E-03
FIBN 5 1 VOFP 2.000000E-03
* AMPLIFYING STAGE
FIP 5 19 VOFP 3.600000E+02
FIN 5 19 VOFN 3.600000E+02
RG1 19 5 3.652997E+06
RG2 19 4 3.652997E+06
CC 19 5 6.000000E-09
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 7.500000E+03
VIPM 28 4 1.500000E+02
HONM 21 27 VOUT 7.500000E+03
VINM 5 27 1.500000E+02
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 20
COUT 3 5 1.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 2.242230E+00
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```
DON 24 19 MDTH 400E-12
VON 24 5 7.922301E-01
.ENDS
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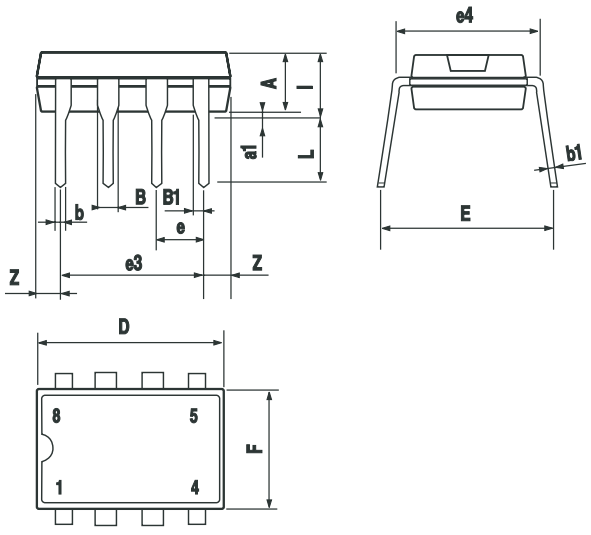
6 Package mechanical data

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

6.1 DIP8 package

Plastic DIP-8 MECHANICAL DATA

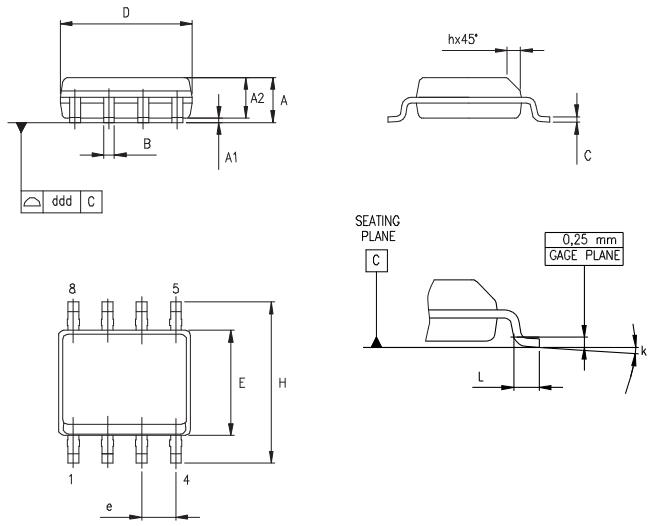
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063



P001F

6.2 SO-8 package

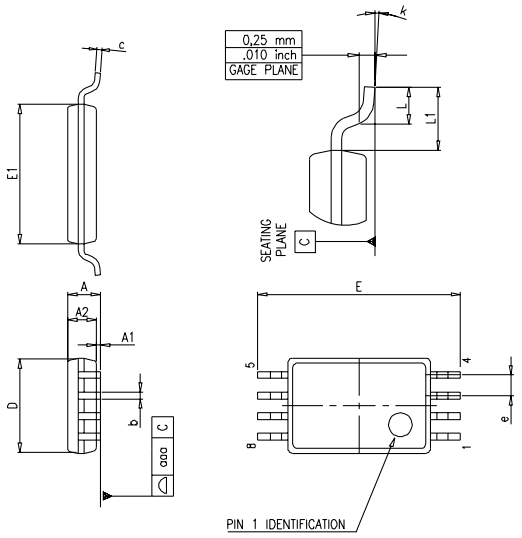
SO-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



6.3 TSSOP8 package

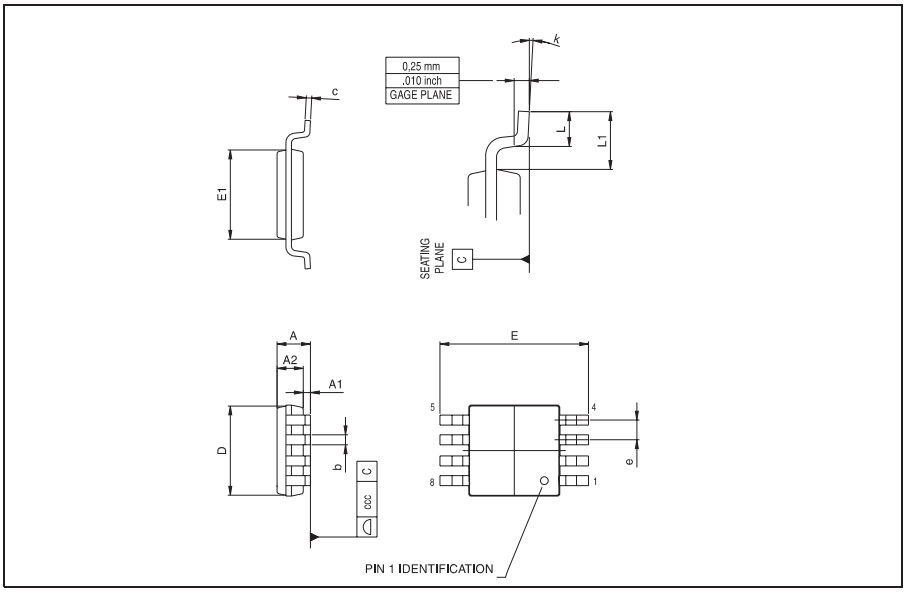
TSSOP8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	



6.4 Mini SO-8 package

miniSO-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.031	0.037
b	0.25	0.33	0.40	0.010	0.13	0.013
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	.0114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



7 Revision history

Table 3. Document revision history

Date	Revision	Changes
Jan. 2002	1	Initial release.
June 2005	2	PPAP references inserted in the datasheet see table*1 Device summary table on page 3*. ESD protection inserted in *Table 1. Absolute maximum ratings on page 4*.
Oct. 2005	3	PPAP part numbers added in table *1 Device summary table on page 3*.
Dec. 2005	4	Pin connections identification added on drawing see page1. Thermal Resistance Junction to Case information added see *Table 1. on page 4*.
Feb. 2006	5	Maximum junction temperature parameter added in *Table 1. on page 4*.
May 2006	6	Minimum slew rate parameter in temperature *Table 2. on page 6*.
Jul. 2006	7	Modified ESD values and added explanation on V_{cc}, V_{id} in *Table 1. on page 4*. Added macromodel information.

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