2Pai Semi

Low Power, 3.0kV rms Dual I²C Isolators

Data Sheet

π220N31/π221N31

FEATURES

- Bidirectional I²C communication
- Ultra-low power consumption
- Supports up to 2MHz operation
- Open-drain interfaces
  - Side 1 outputs with 3.5 mA sink current
  - Side 2 outputs with 35 mA sink current
- 3.0V to 5.5V supply/logic levels
- High common-mode transient immunity: 120 kV/μs typical
- Safety and regulatory approvals：
  - UL certificate number: E494497
    - 3000Vrms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - VDE certificate number: 40053041
    - DIN VDE V 0884-11:2017-01
    - V_{IORM} = 565V peak
- CQC certification per GB4943.1-2011
- AEC-Q100 qualification
- Wide temperature range: -40°C to 125°C
- RoHS-compliant, NB SOIC-8 package

APPLICATIONS

- Isolated I²C, SMBus, PMBus interfaces
- Multilevel I²C interfaces
- Electric and Hybrid-Electric Vehicles
- Open-Drain Networks
- I²C Level Shifting
- Power supplies

GENERAL DESCRIPTION

The π220N31/π221N31 devices are low-power bidirectional isolators compatible with the I²C interface and are based on **iDivider®** technology from 2PaiSemi. These devices have logic input and output buffers that are separated by using a silicon dioxide (SiO_2) barrier. These devices block high voltages and prevent noise currents from entering the control side ground, avoiding circuit interference and damaging sensitive components.

The π220N31/π221N31 devices are based on **iDivider®** technology with functional, performance, size, and power consumption advantages as compared to optocouplers.

The π220N31 provides two bidirectional channels, supporting a complete isolated I²C interface. The π221N31 provides one bidirectional channel and one unidirectional channel for applications where a bidirectional clock is not required. The π221N31 is used in applications that have a single master while the π220N31 is suitable for multi-master applications.

These devices feature independent 3.0V to 5.5V supplies on each side of the isolator. These devices operate from DC to 2MHz at ambient temperatures of -40°C to +125°C.

FUNCTIONAL BLOCK DIAGRAMS

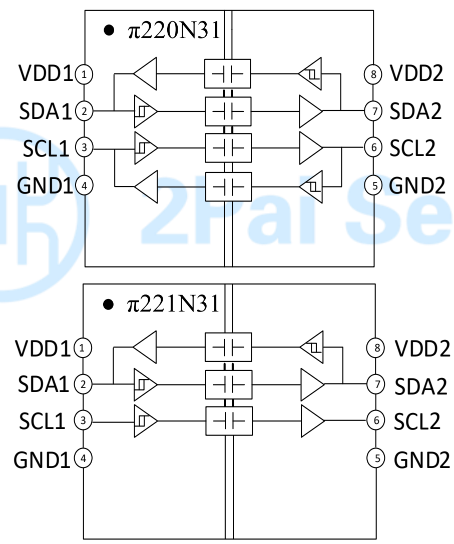

Figure1. π220N31/π221N31 functional Block Diagram

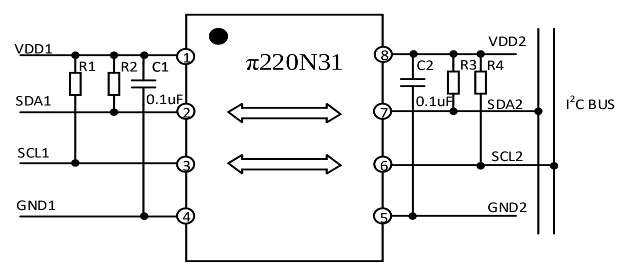

Figure2. π220N31 Typical Application Circuit

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PIN CONFIGURATIONS AND FUNCTIONS

π220N31/π221N31 Pin Function Descriptions

Pin No.	Name	Description
1	VDD1	Supply Voltage for Isolator Side 1.
2	SDA1	Serial data input / output, side 1.
3	SCL1	Serial clock input / output, side 1.
4	GND1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	SCL2	Serial clock input / output, side 2.
7	SDA2	Serial data input / output, side 2.
8	VDD2	Supply Voltage for Isolator Side 2.

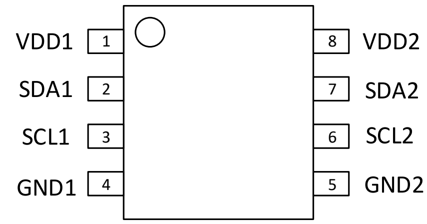


Figure 3. π220N31/π221N31 Pin Configuration

ABSOLUTE MAXIMUM RATINGS

Table 1. Absolute Maximum Ratings[1,2]

Parameter	Rating
Supply Voltages (V_{DD1}-GND_1, V_{DD2}-GND_2)	−0.5 V to +7.0 V
Signal Voltage SDA1/SCL1	−0.5 V to V_{DDx} + 0.5 V
Signal Voltage SDA2/SCL2	−0.5 V to V_{DDx} + 0.5 V
Average Output Current SDA1/SCL1 (I_{O1})	−20 mA to +20 mA
Average Output Current SDA2/SCL2 (I_{O2})	−100 mA to +100 mA
Storage Temperature (T_{ST}) Range	−55°C to +150°C
Maximum junction temperature $T_{J(MAX)}$	+150°C

Notes:

[1] All voltage values here within are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.

[2] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DDx} [1]	3		5.5	V
Input/Output Signal Voltage (V_{SDA1}, V_{SCL1}, V_{SDA2}, V_{SCL2})		0		V_{DDx}[1]	V
Low-level input voltage, side 1	V_{IL1}	0		0.45	V
High-level input voltage, side 1	V_{IH1}	0.7*V_{DD1}		V_{DD1}	V
Low-level input voltage, side 2	V_{IL2}	0		0.3*V_{DD2}	V
High-level input voltage, side 2	V_{IH2}	0.7*V_{DD2}		V_{DD2}	V
Output current, side 1	I_{OL1}	0.5		3.5	mA
Output current, side 2	I_{OL2}	0.5		35	mA
Capacitive load, side 1	C1			40	pF
Capacitive load, side 2	C2			400	pF
Operating frequency	f_{MAX}			2	MHz
Ambient Operating Temperature	T_A	-40		125	°C

Notes:

[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Truth Tables

Table 3. π220N31/π221N31 Truth Table

V_{Ix} Input[1]	V_{DDI} State[1]	V_{DDO} State[1]	V_{Ox} Output[1]
Low	Powered[2]	Powered[2]	Low
High	Powered[2]	Powered[2]	High Impedance
Open[4]	Powered[2]	Powered[2]	High Impedance
Don't Care	Unpowered[3]	Powered[2]	High Impedance
Don't Care	Powered[2]	Unpowered[3]	High Impedance

Notes:
[1] V_{Ix}/V_{Ox} are the input/output signals of a given channel (SDA or SCL). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.
[2] Powered means $V_{DDx} \geq 2.95$ V
[3] Unpowered means $V_{DDx} < 2.30$V
[4] Invalid input condition as an I²C system requires that a pullup resistor to V_{DD} is connected.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Table 4. DC Specifications

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}\pm10\%$ or $5V_{DC}\pm10\%$, $T_A=25°C$, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SIDE 1 LOGIC LEVELS						
Voltage input threshold low, SDA1 and SCL1	V_{ILT1}	470	510	570	mV	
Voltage input threshold high, SDA1 and SCL1	V_{IHT1}	540	580	630	mV	
Voltage input hysteresis	V_{HYST1}	50	70		mV	$V_{IHT1} - V_{ILT1}$
Low-level output voltage, SDA1 and SCL1	V_{OL1}	650	700	800	mV	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5 mA
Low-level output voltage to high-level input voltage threshold difference, SDA1 and SCL1	ΔV_{OIT1}[1]	60	120		mV	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5 mA
SIDE 2 LOGIC LEVELS						
Voltage input threshold low, SDA2 and SCL2	V_{ILT2}	$0.30^* V_{DD2}$		0.42^*V_{DD2}	V	
Voltage input threshold high, SDA2and SCL2	V_{IHT2}	$0.60^* V_{DD2}$		0.66^*V_{DD2}	V	
Voltage input hysteresis	V_{HYST2}	$0.20^* V_{DD2}$	$0.28^* V_{DD2}$		V	$V_{IHT2} - V_{ILT2}$
Low-level output voltage, SDA2 and SCL2	V_{OL2}			0.4	V	0.5 mA ≤ (I_{SDA2} and I_{SCL2}) ≤ 35 mA
BOTH SIDES						
Input leakage currents, SDA1, SCL1, SDA2, and SCL2	$\lvert I_{IN}\rvert$		0.01	10	µA	V_{SDA1}, $V_{SCL1} = V_{DD1}$; V_{SDA2}, $V_{SCL2} = V_{DD2}$
V_{DDx}[3]Undervoltage Rising Threshold	V_{DDxUV+}	2.45	2.75	2.95	V	
V_{DDx}[3]Undervoltage Falling Threshold	V_{DDxUV-}	2.30	2.60	2.80	V	
V_{DDx}[3]Hysteresis	V_{DDxUVH}		0.15		V	

Notes:
[1] $\Delta V_{OIT1} = V_{OL1} - V_{IHT1}$. This is the minimum difference between the output logic low level and the input logic threshold within a given component. This ensures that there is no possibility of the part latching up the bus to which it is connected.
[2] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Table 5. Quiescent Supply Current

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, R1, R2 = Open; C1, C2 = Open (figure 17), unless otherwise noted. Test method refer to Figure 17.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
π220N31 Quiescent Supply Current @ 5V_{DC} Supply	$I_{DD1 (Q)}$		1.7	2.4	mA	VSDA1, VSCL1 = GND1; VSDA2, VSCL2 = GND2
	$I_{DD2 (Q)}$		1.4	2.1	mA	
	$I_{DD1 (Q)}$		1.5	2.3	mA	VSDA1, VSCL1 = VDD1; VSDA2, VSCL2 = VDD2
	$I_{DD2 (Q)}$		1.2	1.8	mA	
π220N31 Quiescent Supply Current @ 3.3V_{DC} Supply	$I_{DD1 (Q)}$		1.5	2.3	mA	VSDA1, VSCL1 = GND1; VSDA2, VSCL2 = GND2
	$I_{DD2 (Q)}$		1.2	1.8	mA	
	$I_{DD1 (Q)}$		1.5	2.3	mA	VSDA1, VSCL1 = VDD1; VSDA2, VSCL2 = VDD2
	$I_{DD2 (Q)}$		1.2	1.8	mA	
π221N31 Quiescent Supply Current @ 5V_{DC} Supply	$I_{DD1 (Q)}$		1.1	1.7	mA	VSDA1, VSCL1 = GND1; VSDA2, VSCL2 = GND2
	$I_{DD2 (Q)}$		1.2	1.8	mA	
	$I_{DD1 (Q)}$		1.2	1.8	mA	VSDA1, VSCL1 = VDD1; VSDA2, VSCL2 = VDD2
	$I_{DD2 (Q)}$		1.2	1.8	mA	
π221N31 Quiescent Supply Current @ 3.3V_{DC} Supply	$I_{DD1 (Q)}$		1.0	1.5	mA	VSDA1, VSCL1 = GND1; VSDA2, VSCL2 = GND2
	$I_{DD2 (Q)}$		1.1	1.7	mA	
	$I_{DD1 (Q)}$		1.1	1.7	mA	VSDA1, VSCL1 = VDD1; VSDA2, VSCL2 = VDD2
	$I_{DD2 (Q)}$		1.1	1.7	mA	

Table 6. Switching Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted. Test method refer to Figure 17.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Output Signal Fall Time SDA1, SCL1	t_{f1}	10	18	30	ns	0.9 V_{DD1} to 0.9 V ; R1 = 1430 Ω,C1 = 40 pF ,@ 5V_{DC} supply
		9	16	28	ns	R1 = 953 Ω, C1 = 40 PF; @ 3.3V_{DC} supply
		6	11	18	ns	0.7 V_{DD1} to 0.3 V_{DD1} ; R1 = 1430 Ω,C1 = 40 pF ,@ 5V_{DC} supply
		6	10	16	ns	R1 = 953 Ω, C1 = 40 PF; @ 3.3V_{DC} supply
Output Signal Fall Time (SDA2, SCL2)	t_{f2}	22	36	45	ns	0.9V_{DD2} to 0.4V; R2 = 143 Ω, C2 = 400 pF, @ 5V_{DC} supply
		20	31	42	ns	R2 = 95.3 Ω,C2 = 400 pF; @ 3.3V_{DC} supply
		9	16	26	ns	0.7 V_{DD2} to 0.3 V_{DD2}; R2 = 143 Ω, C2 = 400 pF, @ 5V_{DC} supply
		8	14	23	ns	R2 = 95.3 Ω,C2 = 400 pF; @ 3.3V_{DC} supply
Low-to-High Propagation Delay, Side 1 to Side 2	t_{pLH1-2}		45	68	ns	0.55 V to 0.7 × V_{DD2}; R1 = 1430 Ω, R2 = 143 Ω, C1, C2 = 10 pF; @ 5V_{DC} supply
			38	57	ns	R1 = 953 Ω, R2 = 95.3 Ω, C1, C2 = 10 pF; @ 3.3V_{DC} supply
High-to-Low Propagation Delay, Side 1 to Side 2	t_{PHL1-2}		67	100	ns	0.7 V to 0.4 V; R1 = 1430 Ω, R2 = 143 Ω, C1, C2 = 10 pF; @ 5V_{DC} supply
			64	96	ns	R1 = 953 Ω, R2 = 95.3 Ω, C1, C2 = 10 pF; @ 3.3V_{DC} supply
Pulse Width Distortion $\lvert t_{pHL1-2} – t_{pLH1-2} \rvert$	PWD_{1-2}		22	32	ns	R1 = 1430 Ω, R2 = 143 Ω, C1, C2 = 10 pF; @ 5V_{DC} supply
			26	39	ns	R1 = 953 Ω, R2 = 95.3 Ω, C1, C2 = 10 pF; @ 3.3V_{DC} supply

Low-to-High Propagation Delay, Side 2 to Side 1	t_{PLH2-1}	44	62	ns	0.4 × V_{DD2} to 0.7 × VDD1; R1 = 1430 Ω, R2 = 143 Ω, C1, C2 = 10 pF; @ $5V_{DC}$ supply
		42	56	ns	R1 = 953 Ω, R2 = 95.3 Ω, C1, C2 = 10 pF; @ $3.3V_{DC}$ supply
High-to-Low Propagation Delay, Side 2 to Side 1	t_{PHL2-1}	52	78	ns	0.4 × V_{DD2} to 0.9 V; R1 = 1430 Ω, R2 = 143 Ω, C1, C2 = 10 pF; @ $5V_{DC}$ supply
		57	86	ns	R1 = 953 Ω,R2 = 95.3 Ω,C1, C2 = 10 pF; @ $3.3V_{DC}$ supply
Pulse Width Distortion $\|t_{PHL2-1} – t_{PLH2-1}\|$	PWD_{2-1}	8	16	ns	R1 = 1430 Ω,R2 = 143 Ω,C1,2 = 10 pF; @ $5V_{DC}$ supply
		15	30	ns	R1 = 953 Ω,R2 = 95.3 Ω,C1, C2 = 10 pF; @ $3.3V_{DC}$ supply
Round-trip propagation delay on Side 1	t_{LOOP1}	104	156	ns	0.4 V to 0.3 × V_{DD1}; R1 = 1430 Ω, R2 = 143 Ω,C1,C2 = 10 pF; @ $5V_{DC}$ supply
		88	132	ns	R1 = 953 Ω,R2 = 95.3 Ω,C1, C2 = 10 pF; @ $3.3V_{DC}$ supply
Common-Mode Transient Immunity[2]	CMTI	120		kV/µs	V_{IN} = V_{DDx}[1] or 0V, V_{CM} = 1000 V.
ESD（HBM - Human body model）	ESD	±6		kV	

Notes:
[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.
[2] See Figure21 for Common-mode transient immunity (CMTI) measurement.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 7. Insulation Specifications

Parameter	Symbol	Value π220N31/π221N31	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	4	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	4	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	4.5	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		21	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 8. Package Characteristics

Parameter	Symbol	Typical Value π220N31/π221N31	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}	10^{11}	Ω	
Capacitance (Input to Output)[1]	C_{I-O}	1.5	pF	@1MHz
Input Capacitance[2]	C_I	7	pF	@1MHz
IC Junction to Ambient Thermal Resistance	$θ_{JA}$	100	°C/W	Thermocouple located at center of package underside

Notes:

[1]The device is considered a 2-terminal device; SOIC-8 Pin 1 - Pin 4 are shorted together as the one terminal, and SOIC-8 Pin 5 - Pin 8 are shorted together as the other terminal.
[2]Testing from the input signal pin to ground.

REGULATORY INFORMATION

See Table 9 for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 9. Regulatory

UL	VDE	CQC
Recognized under UL 1577 Component Recognition Program[1]	DIN VDE V 0884-11:2017-01[2] Basic insulation, V_{IORM} = 565V peak, V_{IOSM} = 3615 V peak	Certified under CQC11-471543-2012
Single Protection, 3000 V rms Isolation Voltage		GB4943.1-2011
		Basic insulation at 500 V rms (707 V peak) working voltage Reinforced insulation at 250 V rms (354 V peak)
File (E494497)	File (40053041)	File (CQC20001260211)

Notes:
[1]In accordance with UL 1577, each π220N31/π221N31 is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec.
[2]In accordance with DIN V VDE V 0884-11, each π220N31/π221N31 is proof tested by applying an insulation test voltage ≥ 848V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-11 approval.

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The * marking on packages denotes DIN V VDE V 0884-11 approval.

Table 10. VDE Insulation Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic π220N31/π221N31	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive peak isolation voltage		V_{IORM}	565	V peak
Input to Output Test Voltage, Method B1	V_{IORM} × 1.5 = $V_{pd\ (m)}$, 100% production test, tini = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	848	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	678	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		678	V peak
Highest Allowable Overvoltage		V_{IOTM}	4200	V peak
Surge Isolation Voltage Basic	Basic insulation, 1.2 µs rise time, 50 µs, 50% fall time , VTEST = 1.3 × VIOSM (qualification)[1]	V_{IOSM}	3615	V peak

Surge Isolation Voltage Reinforced	Reinforced insulation, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}		V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Maximum Junction Temperature		T_S	150	°C
Maximum Power Dissipation at 25°C		P_S	1.25	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>10^9	Ω

Notes:
[1]In accordance with DIN V VDE V 0884-11, π220N31/π221N31 is proof tested by applying a surge isolation voltage 4700 V.

Typical Thermal Characteristic

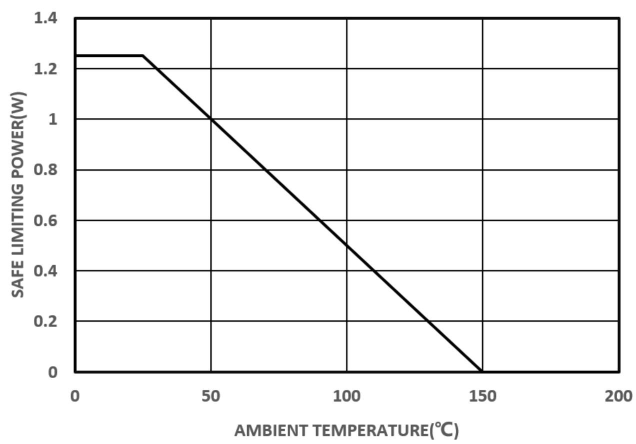


Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE

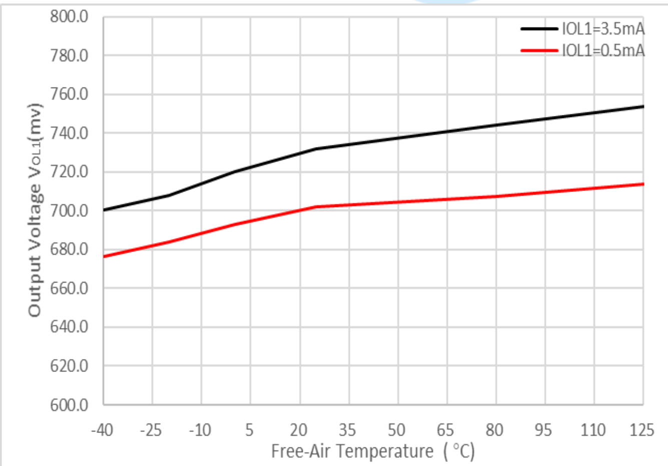


Figure 5. Side 1: Output Low Voltage vs Free-Air Temperature

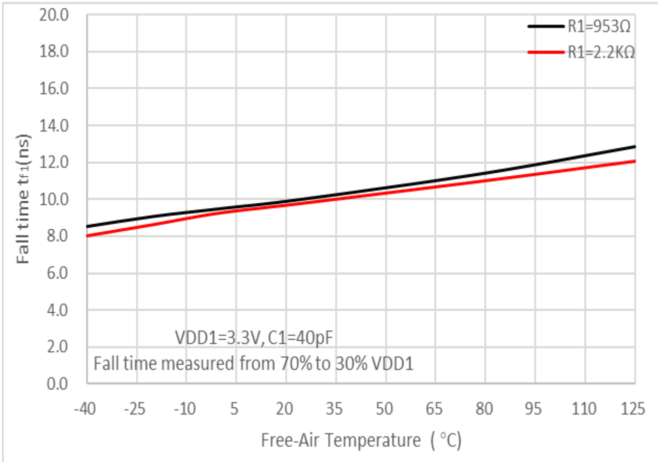


Figure 6. Side 1: Output Fall Time vs Free-Air Temperature

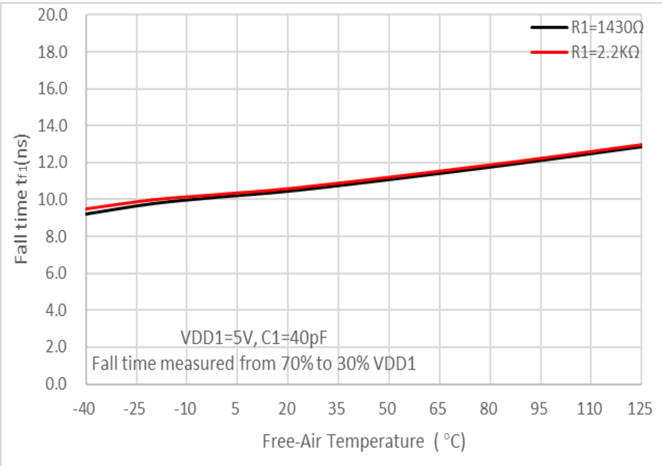


Figure 7. Side 1: Output Fall Time vs Free-Air Temperature

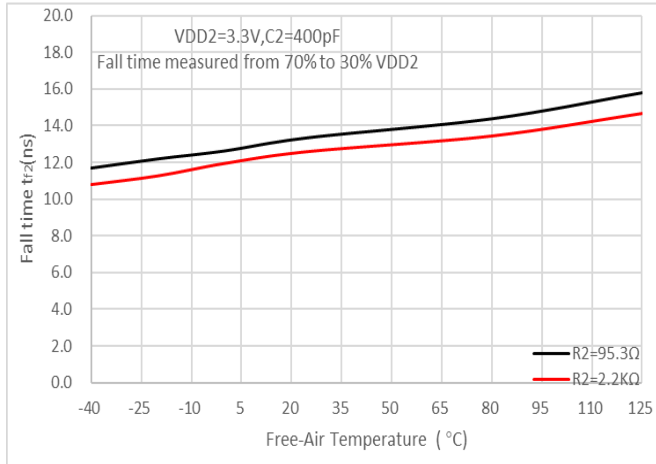


Figure 8. Side 2: Output Fall Time vs Free-Air Temperature

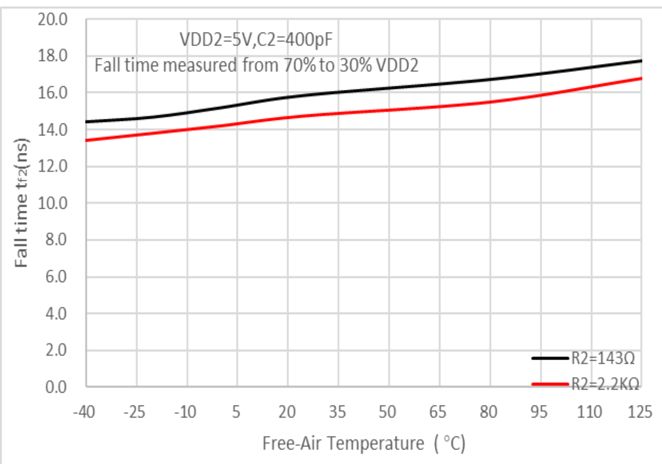


Figure 9. Side 2: Output Fall Time vs Free-Air Temperature

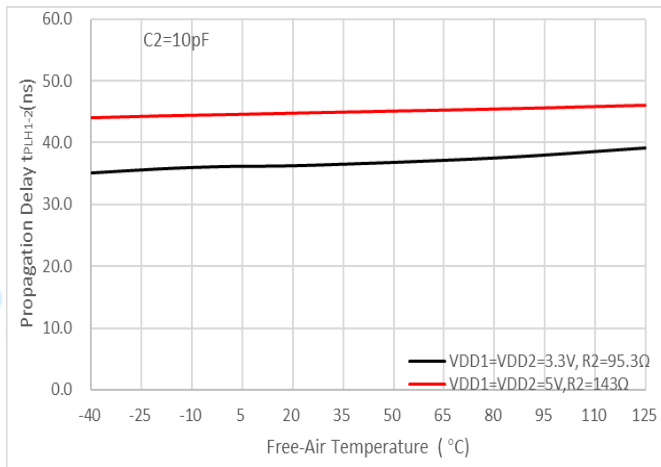


Figure 10. t_{PLH1-2} Propagation Delay vs Free-Air Temperature

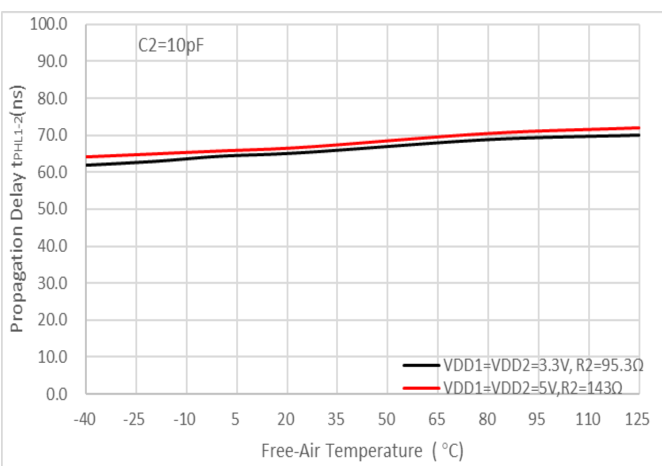


Figure11. t_{PHL1-2} Propagation Delay vs Free-Air Temperature

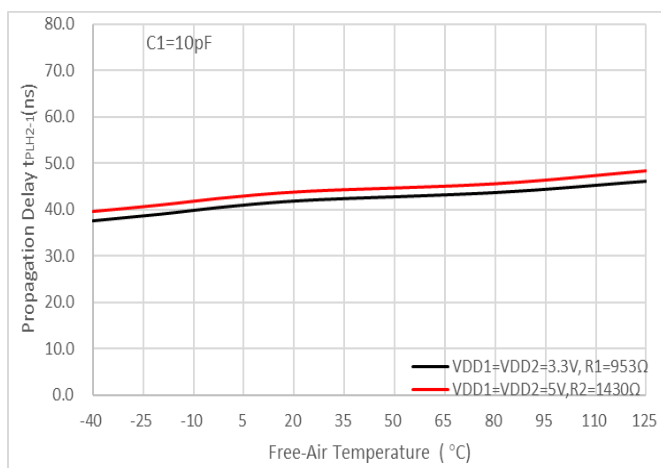


Figure12. t_{PLH1-2} Propagation Delay vs Free-Air Temperature

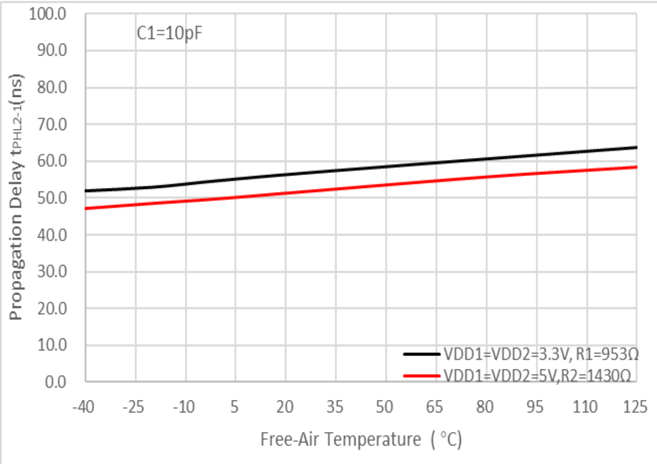


Figure13. t_{PHL2-1} Propagation Delay vs Free-Air Temperature

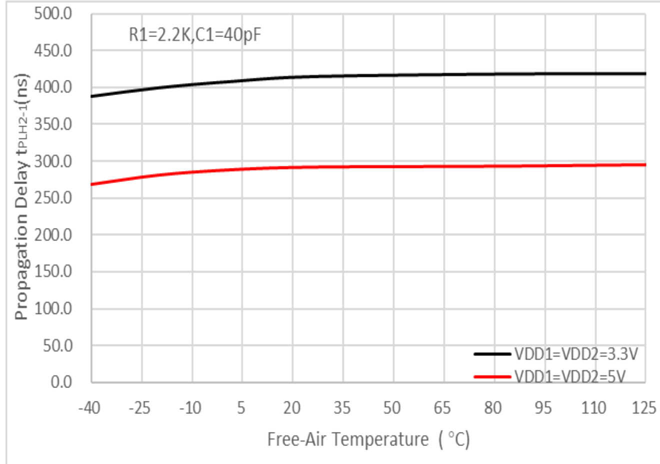


Figure14. t_{PLH2-1} Propagation Delay vs Free-Air Temperature

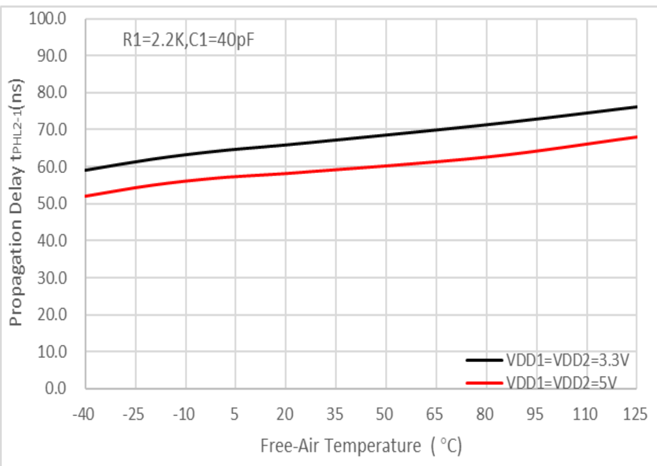


Figure15. t_{PHL2-1} Propagation Delay vs Free-Air Temperature

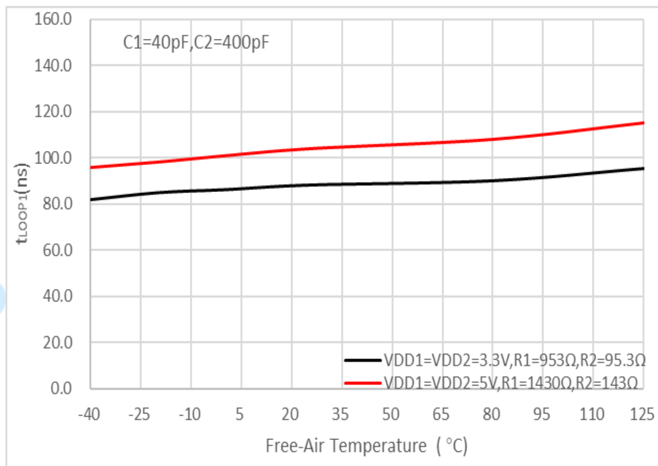


Figure16. t_{LOOP1} vs Free-Air Temperature

PARAMETER MEASUREMENT INFORMATION

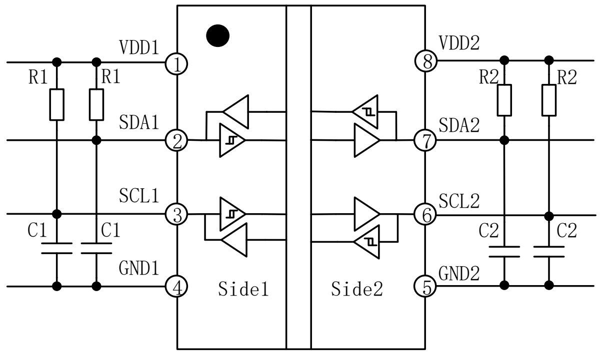


Figure 17. Test Diagram

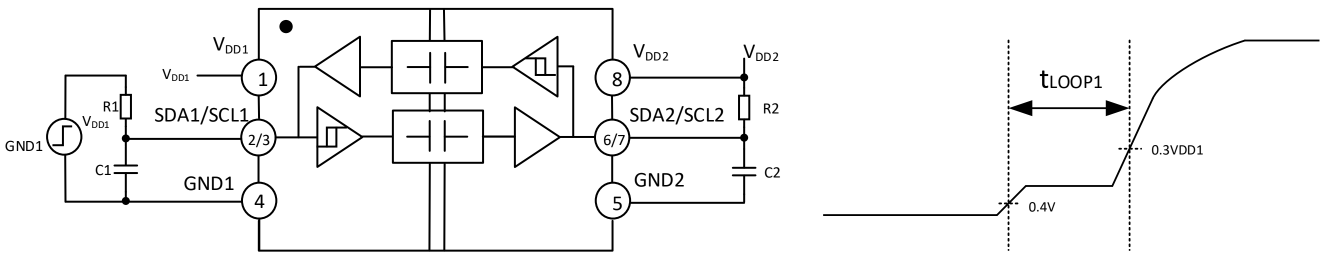


Figure 18. t_{Loop1} Setup and Timing Diagram

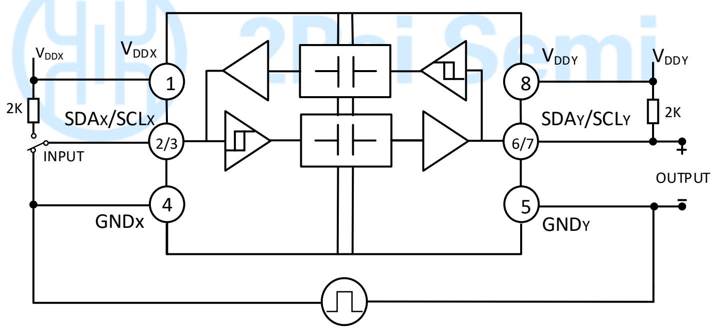


Figure 19. Common-Mode Transient Immunity Test Circuit

APPLICATIONS INFORMATION

Overview

The inter-integrated circuit (I^2C) bus is a single-ended, two wire bus for efficient inter-IC communication and is used in a wide range of applications. The I^2C bus is used for communication between multiple masters or a single master and slaves. The master device controls the serial clock line (SCL) and data is bidirectional transferred on the serial data line (SDA) between master and slaves. The I^2C bus can theoretically add up to 112 communication nodes, however, the number of nodes will increase the load capacitance on the bus, thereby limiting the communication distances and communication speeds. In applications, tradeoffs are often made between communication speeds, bus length, and number of nodes based on actual conditions.

The I^2C bus supports data transmission in four speeds: standard mode (up to 100Kbps), fast mode (up to 400Kbps), fast mode plus (up to 1Mbps), and high-speed mode (up to 3.4Mbps). The π220N31/π221N31 devices support all the above four communication modes.

FUNCTIONAL DESCRIPTION

The π220N31/π221N31 devices are low-power bidirectional isolators compatible with the I^2C interface and are based on **iDivider®** technology from 2PaiSemi. These devices have logic input and output buffers that are separated by using a silicon dioxide (SiO_2) barrier. These devices block high voltages and prevent noise currents from entering the control side ground, avoiding circuit interference and damaging sensitive components. Each channel output of the π220N31/π221N31 devices is made open-drain to comply with the open-drain technology of I^2C. Serial data line (SDA)and serial clock line (SCL) need to add pull-up resistors to ensure normal operation of the system. It is recommended that side 1 of the I^2C isolator be connected to the processor and sides 2 to the bus when there are multiple nodes on the I^2C bus as side 2 support up to 400 pF capacitance load.

The π220N31 devices feature two bidirectional channels that have open-drain outputs, As shown in Figure 20. As a logic low on one side causes the corresponding pin on the other side to be pulled low, to avoid data-latching within the device, The output logic low (VOL1)voltages of SDA1 and SCL1 are at least 60mV higher than the input threshold high (VIHT1) of SDA1 and SCL1, As shown in Figure 21.

Because the Side 2 logic levels/thresholds are standard I^2C values, multiple π220N31/π221N31 devices connected to a bus by their Side 2 pins can communicate with each other and with other I^2C compatible devices. However, because the Side 1 pin has a modified output level/ input threshold, this side of the π220N31/π221N31 can communicate only with devices that conform to the I^2C standard.

The output low voltages of π220N31/π221N31 devices are guaranteed for sink currents of up to 35mA for side 2, and 3.5mA for side 1.

To enhance system reliability, it is recommended to connect the node with larger load capacitance and longer wires on side 2 for point-to-point communication.

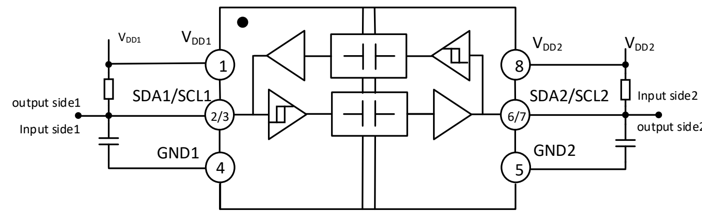


Figure 20. π220N31 system operation diagram

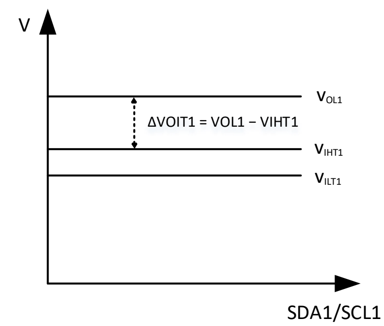


Figure 21. π220N31/ π221N31 side 1 voltage Diagram

TYPICAL APPLICATION DIAGRAM

Figure 22 shows a typical application circuit including the pull-up resistors required for both Side 1 and Side 2. Bypass capacitors with values from 0.1µF to 10µF are required between V_{DD1} and GND1 and between V_{DD2} and GND2. To enhance the robustness of a design, the user may connect a resistor (50-200 Ω) in series between R2 and C1 and between R3 and C2 if the system is excessively noisy.

The π220N31/π221N31 are designed for operation at speeds up to 2 MHZ. Due to the limited current available on side 1 and side2, operation at 2MHZ limits the capacitance that can be driven at the minimum pull-up value to 40pF and 400pF.

Most applications operate at 100 kbps in standard mode or 400 kbps in fast mode. At these lower operating speeds, the limitation on the load capacitance can be significantly relaxed. If larger values for the pull up resistor are used, the maximum supported capacitance must be scaled down proportionately so that the rise time does not increase beyond the values required by the standard.

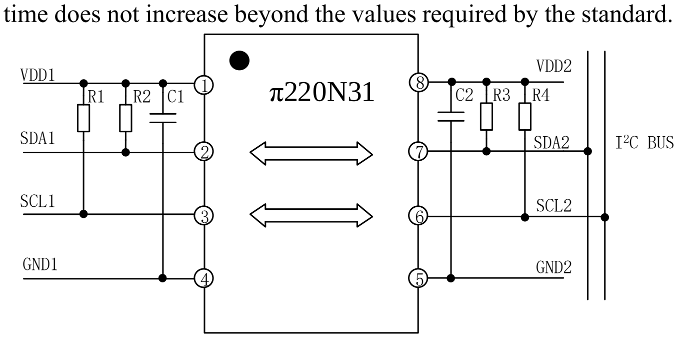
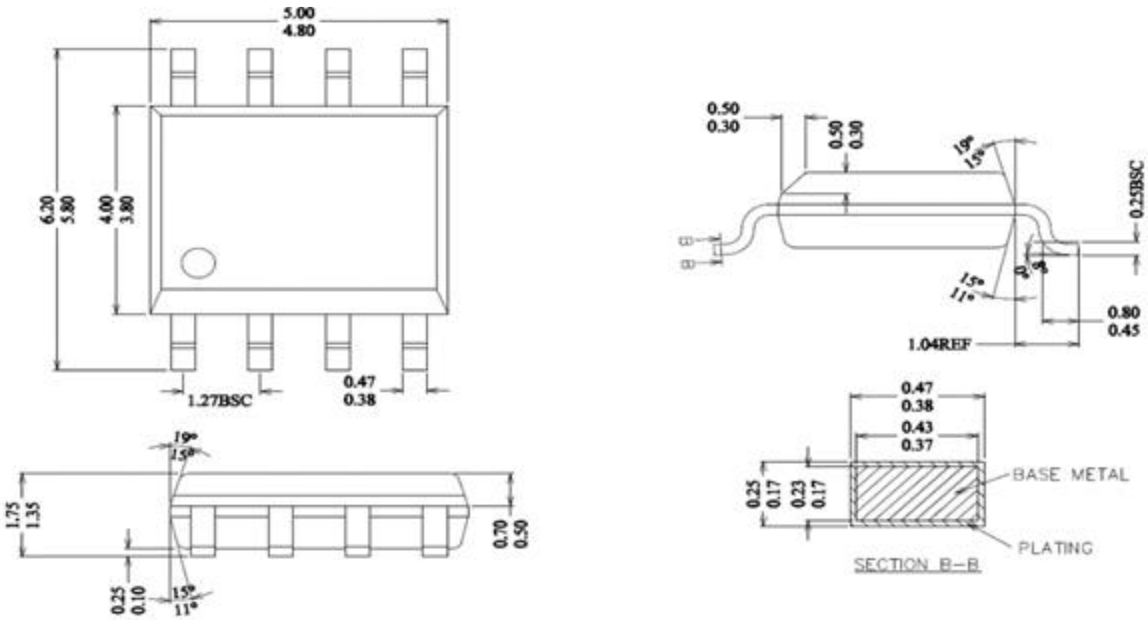


Figure 22. Typical Isolated I²C Interface Using the π220N31

OUTLINE DIMENSIONS



Notes:

ALL DIMENSIONS REFER TO JEDEC STANDARD MS—012 AA

DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

Figure 23. 8-Lead Narrow Body SOIC [NB SOIC-8] *Outline Package – dimension unit(mm)*

Land Patterns

8-Lead Narrow Body SOIC [NB SOIC-8]

The figure below illustrates the recommended land pattern details for the π1xxxxx in an 8-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

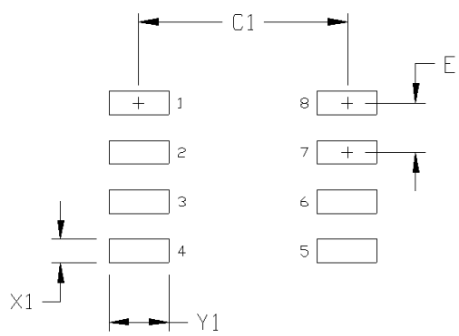


*Figure 24.*8-Lead Narrow Body SOIC [NB SOIC-8] Land Pattern

Table 11.8-Lead Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	5.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.55	mm

Note：

1.This land pattern design is based on IPC -7351.

2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

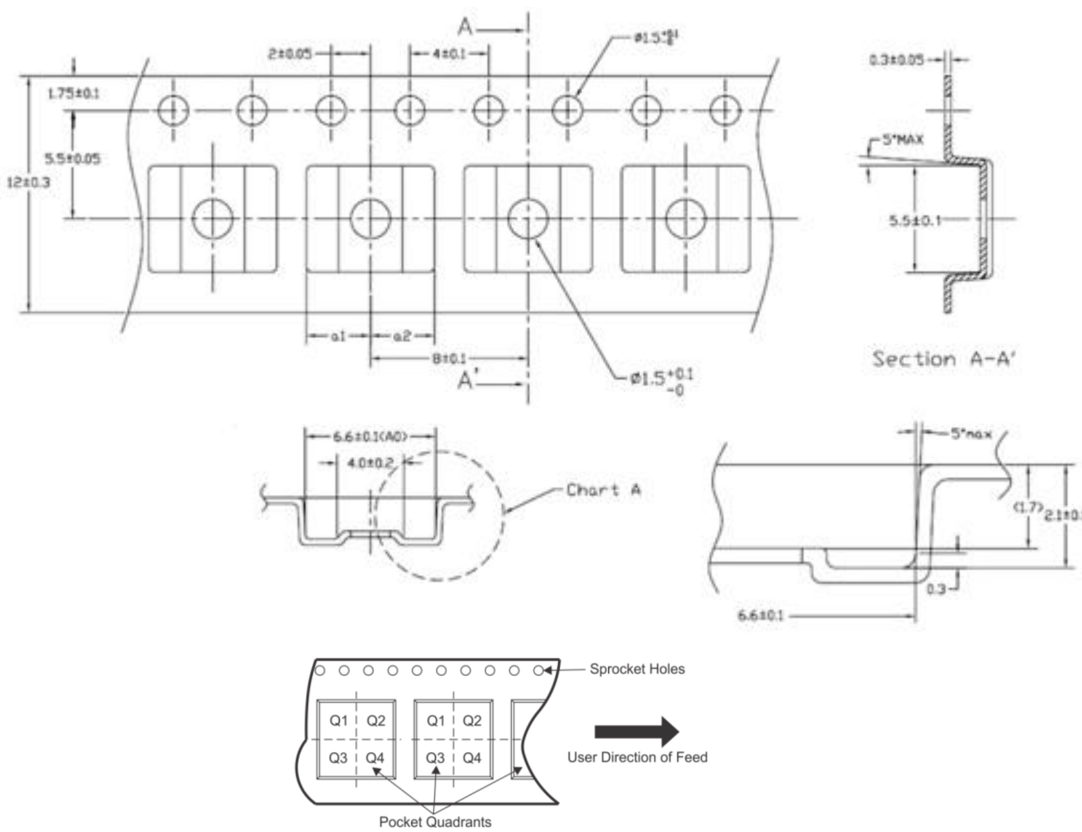
Top Marking

Line 1	π1xxxxxx=Product name
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXX, no special meaning

*Figure 25.*Top Marking

REEL INFORMATION

8-Lead Narrow Body SOIC [NB SOIC-8]



Note：The Pin 1of the chip is in the quadrant Q1

Figure 26. 8-Lead Narrow Body SOIC [NB SOIC-8] Reel Information– *dimension unit(mm)*

ORDERING GUIDE

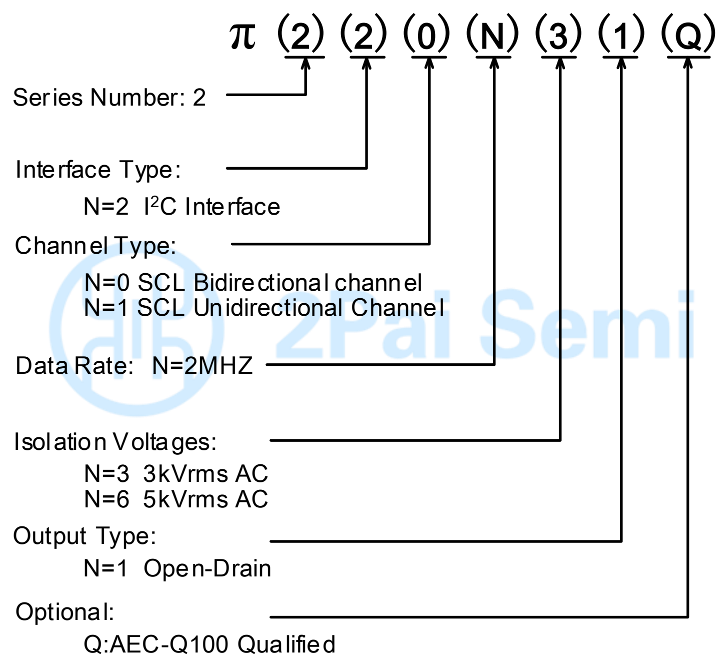
Table 11. ORDERING GUIDE

Model Name[1]		Temperature Range	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Isolation Rating (kV rms)	Maximum Data Rate (MHZ)	Package Description	MSL Peak Temp [2]	MOQ/ Quantity per reel[3]
π220N31	Pai220N31	−40°C to +125°C	2	2	3	2	NB SOIC-8	Level-3-260C-168 HR	4000
π221N31	Pai221N31	−40°C to +125°C	2	1	3	2	NB SOIC-8	Level-3-260C-168 HR	4000

Note：

1. Pai2xxxxx is equals to π2xxxxx in the customer BOM
2. MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
3. MOQ, minimum ordering quantity.

PART NUMBER NAMED RULE



Notes:
Pai22xxxx is equals to π22xxxx in the customer BOM

Figure 27. Part Number Named Rule

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REVISION HISTORY

Revision	Date	Page	Change Record
1.0	2020/02/24	All	Initial version
1.1	2021/05/17	Page6	Changed Regulatory Information