Freescale Semiconductor
Addendum

Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

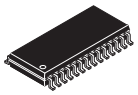
Freescale Semiconductor
Data Sheet: Technical Data

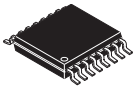
An Energy Efficient Solution by Freescale

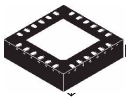
Document Number: MC9S08QB8
Rev. 3, 3/2009

RoHS

MC9S08QB8


28 SOIC
Case 751F


16-Pin TSSOP
Case 948F


24 QFN
Case 1982-01

MC9S08QB8 Series

Covers: MC9S08QB8 and MC9S08QB4

Features

- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 20 MHz CPU at 3.6 V to 1.8 V across temperature range of –40 °C to 85 °C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Up to 8 KB flash memory read/program/erase over full operating voltage and temperature
  - Up to 512 bytes random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two very low power stop modes
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
  - Low power run
  - Low power wait
  - 6 µs typical wakeup time from stop3 mode
  - Typical stop current of 250 nA at 3 V, 25 °C
- Clock Source Options
  - Oscillator (XOSC) — Very low-power, loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1 MHz to 10 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
  - **ADC** — 8-channel, 12-bit resolution; 2.5 µs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V.
  - **ACMP** — Analog comparator with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; output can be tied internally to TPM input capture; operation in stop3
  - **TPM** — One 1-channel timer/pulse-width modulator (TPM) module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; ACMP output can be tied internally to input capture
  - **MTIM** — 8-bit modulo timer module with optional prescaler
  - **RTC** — (Real-time counter) 8-bit modulo counter with binary or decimal based prescaler; external clock source for precise time base, time-of-day, calendar or task scheduling functions; free running on-chip low power oscillator (1 kHz) for cyclic wakeup without external components; runs in all MCU modes
  - **SCI** — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wakeup on active edge
  - **KBI** — 8-pin keyboard interrupt with selectable edge and level detection modes
- Input/Output
  - 22 GPIOs and one input-only and one output-only pin.
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins except PTA5.
- Package Options
  - 28-pin SOIC, 24-pin QFN, 16-pin TSSOP

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
1	10/22/2008	Initial public released.
2	12/17/2008	Completed all the TBDs in Table 8.
3	3/6/2009	Corrected the 24-pin QFN package information. Changed V_{DDAD} and V_{SSAD} to V_{DDA} and V_{SSA} separatedly. In Table 7, updated the $\|I_{In}\|$, $\|I_{OZ}\|$ and added $\|I_{OZTOT}\|$. In Table 11, updated the DCO output frequency range-trimmed, and updated some of the symbols.

Related Documentation

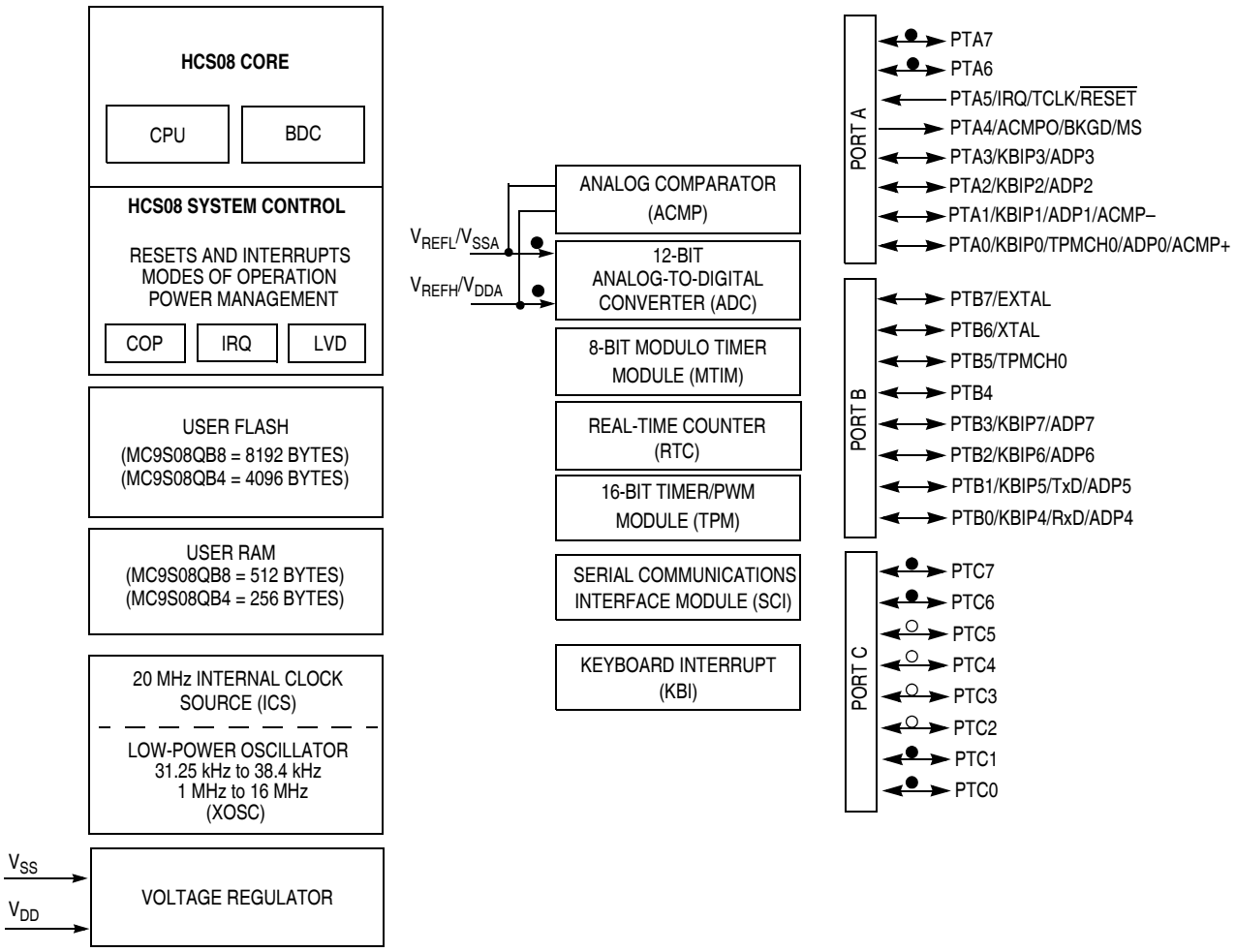
Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08QB8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram shows the structure of the MC9S08QB8 MCU.



○ pins not available on 24-pin or 16-pin packages

● pins not available on 16-pin package

[1] V_{DDA}/V_{REFH} and V_{SSA}/V_{REFL} are double bonded to V_{DD} and V_{SS} respectively in16-pin package.

Figure 1. MC9S08QB8 Series Block Diagram

2 Pin Assignments

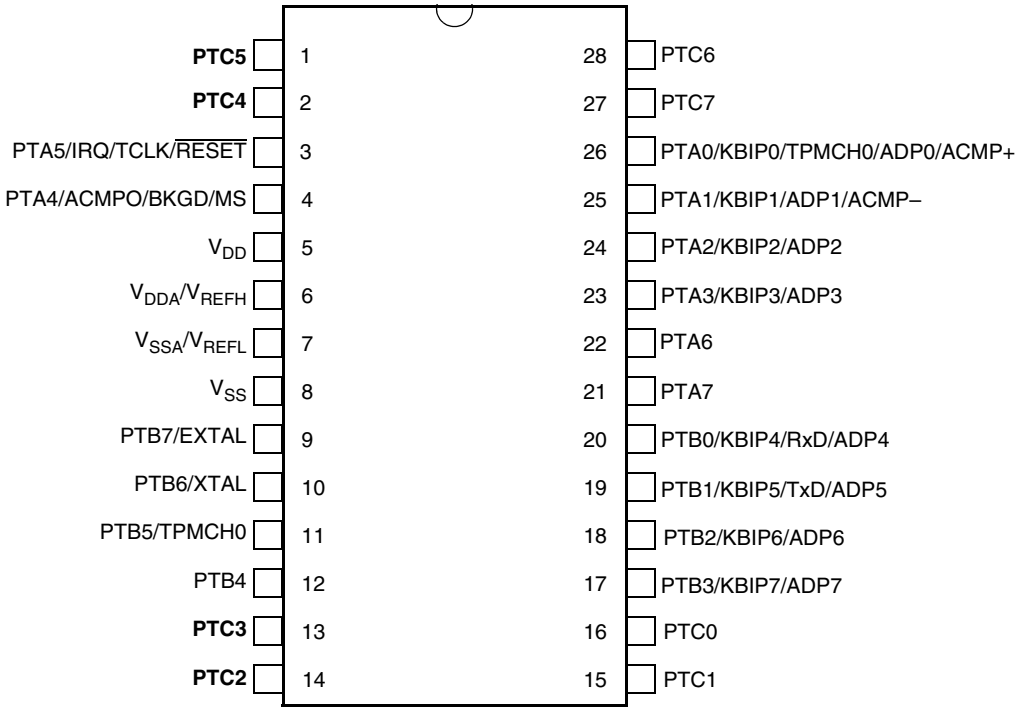
This chapter shows the pin assignments for the MC9S08QB8 series devices.

Table 1. Pin Availability by Package Pin-Count

Pin Number			<-- Lowest **Priority** --> Highest				
28	**24**	**16**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	—	—	PTC5				
2	—	—	PTC4				
3	23	1	PTA5	IRQ	TCLK	$\overline{\text{RESET}}$	
4	24	2	PTA4	ACMPO	BKGD	MS	
5	1	3					V_{DD}
6	2	—					V_{DDA}/V_{REFH}
7	3	—					V_{SSA}/V_{REFL}
8	4	4					V_{SS}
9	5	5	PTB7				EXTAL
10	6	6	PTB6				XTAL
11	7	7	PTB5	TPMCH0[1]			
12	8	8	PTB4				
13	—	—	PTC3				
14	—	—	PTC2				
15	9	—	PTC1				
16	10	—	PTC0				
17	11	9	PTB3	KBIP7		ADP7	
18	12	10	PTB2	KBIP6		ADP6	
19	13	11	PTB1	KBIP5	TxD	ADP5	
20	14	12	PTB0	KBIP4	RxD	ADP4	
21	15	—	PTA7				
22	16	—	PTA6				
23	17	13	PTA3	KBIP3		ADP3	
24	18	14	PTA2	KBIP2		ADP2	
25	19	15	PTA1	KBIP1		ADP1[2]	ACMP–[2]
26	20	16	PTA0	KBIP0	TPMCH0	ADP0[2]	ACMP+[2]
27	21	—	PTC7				
28	22	—	PTC6				

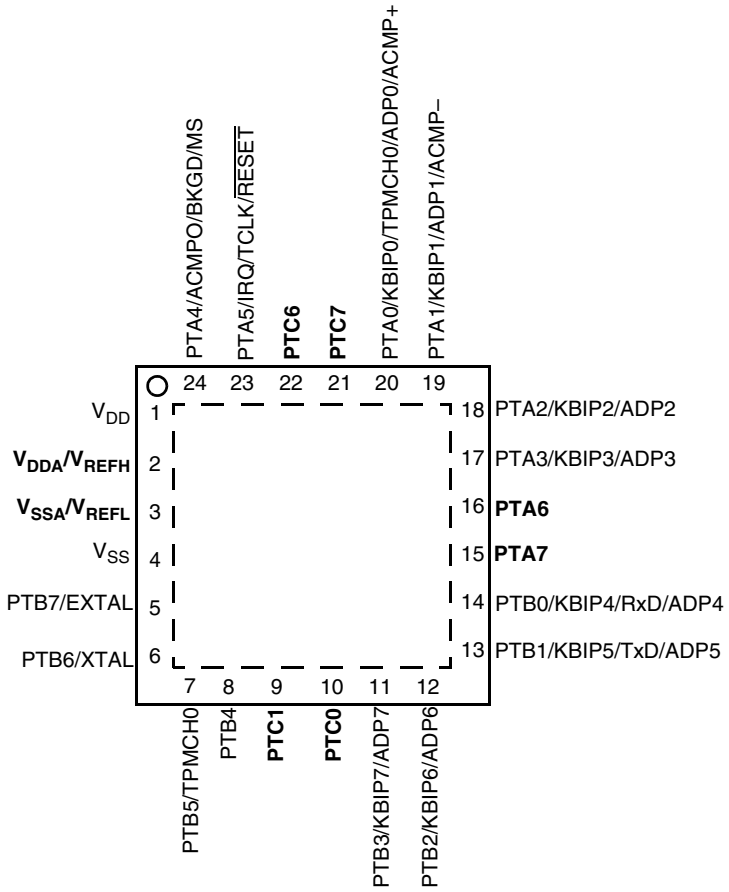
1 TPMCH0 pin can be repositioned using at PTB5 TPMCH0PS in SOPT2, default reset location is PTA0.

2 If ADC and ACMP are enabled, both modules will have access to the pin.



Pins shown in bold type are lost in the next lower pin count package.

Figure 2. MC9S08QB8 Series in 28-Pin SOIC Package



Pins shown in bold type are lost in the next lower pin count package.

Figure 3. MC9S08QB8 Series in 24-Pin QFN Packages

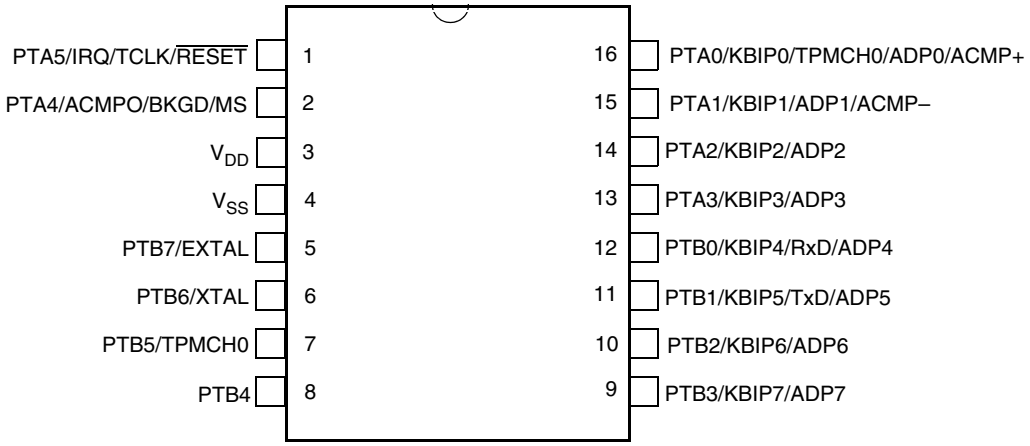


Figure 4. MC9S08QB8 Series in 16-Pin TSSOP Package

3 Electrical Characteristics

3.1 Introduction

This chapter contains electrical and timing specifications for the MC9S08QB8 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_{JM}	95	°C
Thermal resistance 28-pin SOIC	θ_{JA}	70	°C/W
Thermal resistance 24-pin QFN		92	°C/W
Thermal resistance 16-pin TSSOP		129	°C/W

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85°C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min	Typical[1]	Max	Unit
1	P	Operating Voltage		V_{DD}	—	1.8	—	3.6	V
2	C	Output high voltage	All I/O pins, low-drive strength	V_{OH}	V_{DD} > 1.8 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	V
	P		All I/O pins, high-drive strength		V_{DD} > 2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C				V_{DD} > 1.8V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	
3	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	V_{OUT} < V_{DD}	0	—	–80	mA
4	C	Output low voltage	All I/O pins, low-drive strength	V_{OL}	V_{DD} > 1.8 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P		All I/O pins, high-drive strength		V_{DD} > 2.7 V, I_{Load} = 10 mA	—	—	0.5	
	C				V_{DD} > 1.8 V, I_{Load} = 3 mA	—	—	0.5	
5	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	V_{OUT} > V_{SS}	0	—	80	mA
6	P	Input high voltage	all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V
	C				V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	
7	P	Input low voltage	all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C				V_{DD} > 1.8 V	—	—	0.30 x V_{DD}	
8	C	Input hysteresis	all digital inputs	V_{hys}	—	0.06 x V_{DD}	—	—	mV
9	P	Input leakage current	all input only pins (Per pin)	$\|I_{In}\|$	V_{In} = V_{DD} or V_{SS}	—	—	200	nA
10	P	Hi-Z (off-state) leakage current	all input/output (per pin)	$\|I_{OZ}\|$	V_{In} = V_{DD} or V_{SS}	—	—	200	nA

Table 7. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typical[1]	Max	Unit
10	C	Total leakage combined for all inputs and Hi-Z pins — All input only and I/O	$\lvert I_{OZTOT} \rvert$	$V_{In} = V_{DD}$ or V_{SS}	—	—	2	μA
11	P	Pullup, Pulldown resistors — all digital inputs except PTA5/IRQ/TCLK/$\overline{\text{RESET}}$, when enabled	R_{PU}, R_{PD}	—	17.5	—	52.5	kΩ
12	C	Pullup, Pulldown resistors — PTA5/IRQ/TCLK/$\overline{\text{RESET}}$, when enabled[2]	R_{PU}, R_{PD}	—	17.5	—	52.5	kΩ
13	D	DC injection current [3, 4, 5] — Single pin limit	I_{IC}	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	–0.2	—	0.2	mA
		DC injection current [3, 4, 5] — Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
14	C	Input Capacitance, all pins	C_{In}	—	—	—	8	pF
15	C	RAM retention voltage	V_{RAM}	—	—	0.6	1.0	V
16	C	POR re-arm voltage[6]	V_{POR}	—	0.9	1.4	2.0	V
17	D	POR re-arm time	t_{POR}	—	10	—	—	μs
18	P	Low-voltage detection threshold	V_{LVD}	V_{DD} falling V_{DD} rising	1.80 1.88	1.84 1.92	1.88 1.96	V
19	P	Low-voltage warning threshold	V_{LVW}	V_{DD} falling V_{DD} rising	2.08	2.14	2.26	V
20	C	Low-voltage inhibit reset/recover hysteresis	V_{hys}	—	—	80	—	mV
21	P	Bandgap Voltage Reference[7]	V_{BG}	—	1.15	1.17	1.18	V

1 Typical values are measured at 25 °C. Characterized, not tested

2 The specified resistor value is the actual value internal to the device. The pullup or pulldown value may appear lower when measured externally on the pin.

3 All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 Maximum is highest voltage that POR is guaranteed.

7 Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C

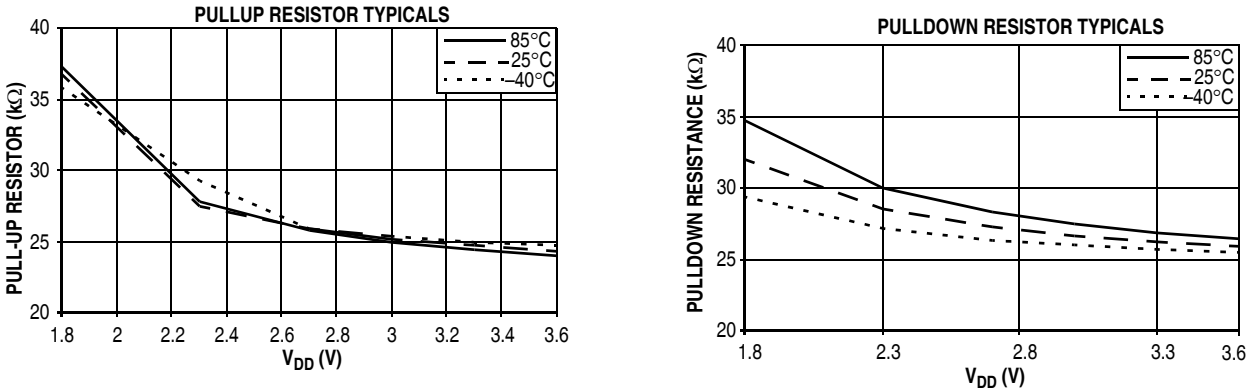


Figure 5. Pullup and Pulldown Typical Resistor Values (V_{DD} = 3.0 V)

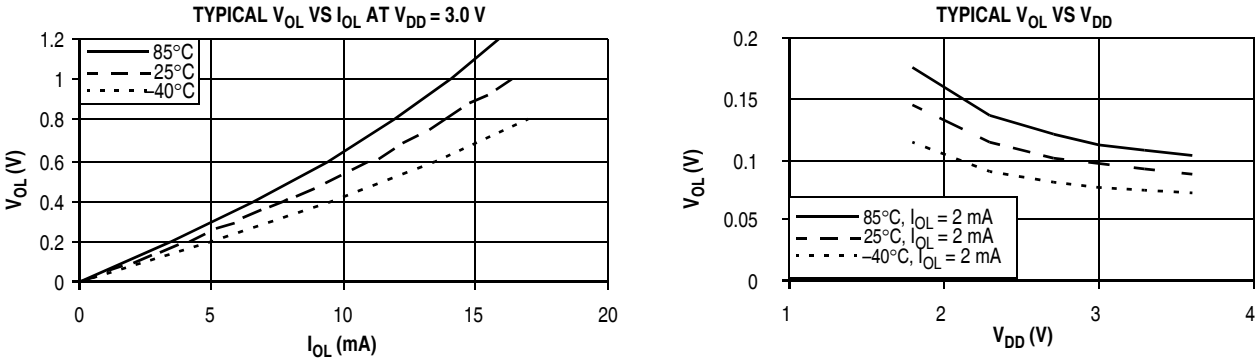


Figure 6. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

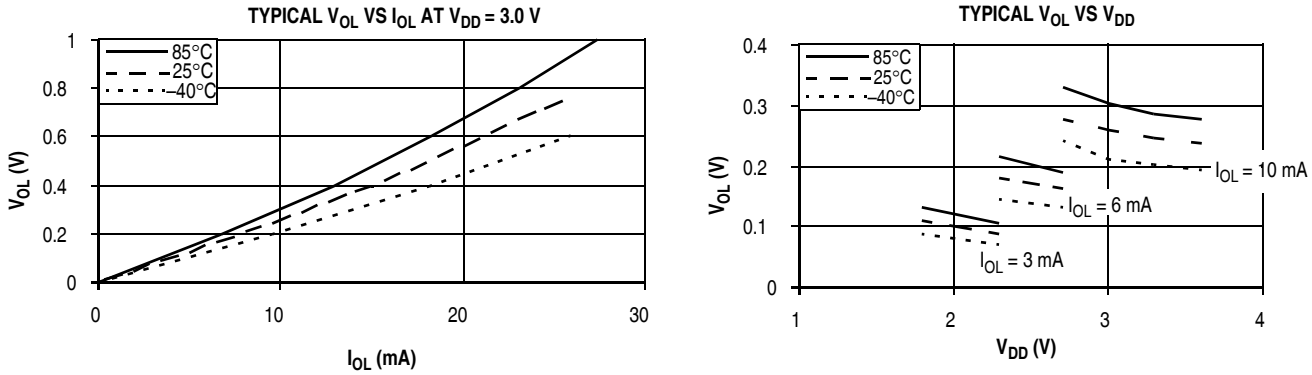


Figure 7. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

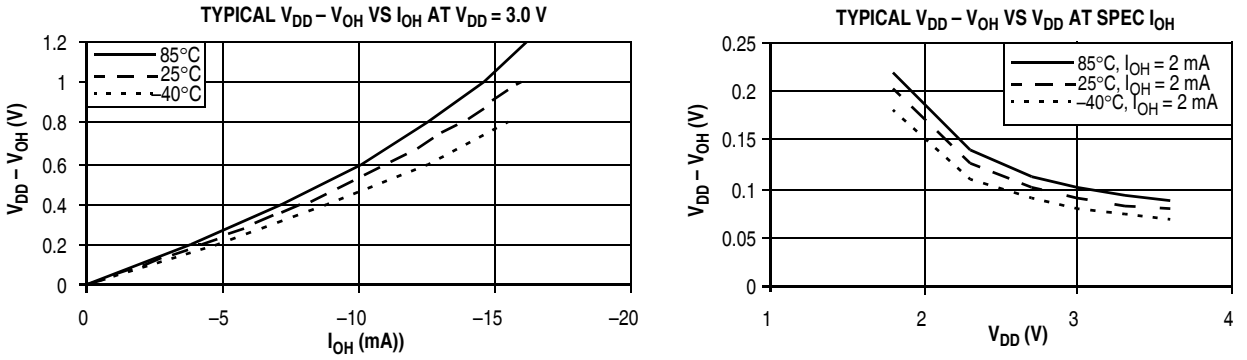


Figure 8. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

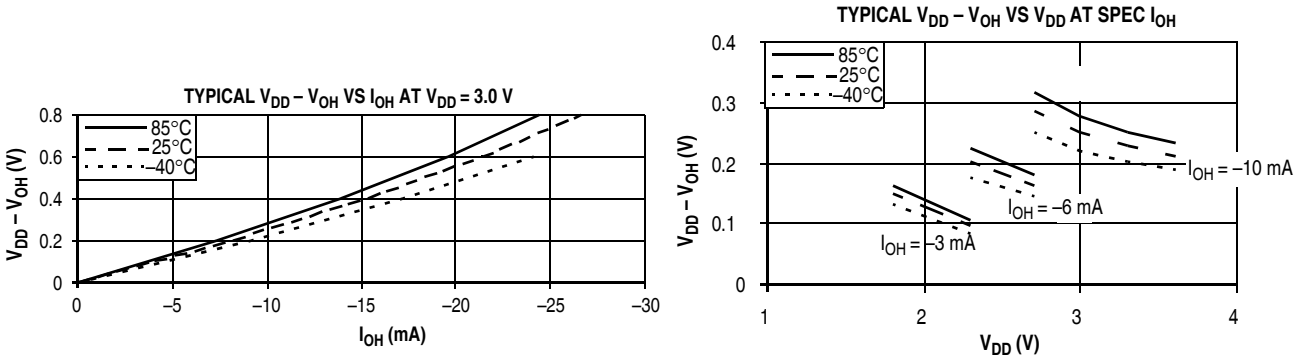


Figure 9. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	10 MHz	3	5.60	6	mA	–40 to 85°C
	T			1 MHz		0.80	—		
2	T	Run supply current FEI mode, all modules off	RI_{DD}	10 MHz	3	3.60	—	mA	–40 to 85°C
	T			1 MHz		0.75	—		
3	T	Run supply current LPRS=0, all modules off	RI_{DD}	16 kHz FBILP	3	165	—	µA	–40 to 85°C
	T			16 kHz FBELP		105	—		
4	T	Run supply current LPRS=1, all modules off	RI_{DD}	16 kHz FBELP	3	7.3	—	µA	–40 to 85°C
5	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	10 MHz	3	570	—	µA	–40 to 85°C
	T			1 MHz		290	—		
6	T	Wait mode supply current LPRS = 1, all mods off	WI_{DD}	16 kHz FBELP	3	1	—	µA	–40 to 85°C
7	P	Stop2 mode supply current	$S2I_{DD}$	—	3	0.25	0.65	µA	–40 to 25°C
	C			—		0.5	0.8		70°C
	P			—		1	2		85°C
	C			—	2	0.2	0.5		–40 to 25°C
	C			—		0.3	0.6		70°C
	C			—		0.7	1.6		85°C
8	P	Stop3 mode supply current no clocks active	$S3I_{DD}$	—	3	0.45	0.80	µA	–40 to 25°C
	C			—		1	1.8		70°C
	P			—		3	5.8		85°C
	C			—	2	0.3	0.6		–40 to 25°C
	C			—		0.8	1.5		70°C
	C			—		2.5	5.0		85°C

[1] Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

Table 9. Stop Mode Adders

Num	C	Parameter	Condition	Temperature				Units
				–40°C	25°C	70°C	85°C	
1	T	LPO	—	50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN[1]	—	63	70	77	81	µA

Table 9. Stop Mode Adders (continued)

Num	C	Parameter	Condition	Temperature				Units
				–40°C	25°C	70°C	85°C	
4	T	RTC	Does not include clock source current	50	75	100	150	nA
5	T	LVD[1]	LVDSE = 1	90	100	110	115	µA
6	T	ACMP[1]	Not using the bandgap (BGBE = 0)	18	20	22	23	µA
7	T	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	106	114	120	µA

[1] Not available in stop2 mode.

3.8 External Oscillator (XOSC) Characteristics

Reference Figure 10 and Figure 11 for crystal or resonator circuits.

Table 10. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1, C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range (RANGE = 1, HGO = X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high gain High range, low power High range, high gain	 t_{CSTL} t_{CSTH}	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	— —	20 20	MHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.
2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
3 See crystal or resonator manufacturer's recommendation.
4 Proper PC board layout procedures must be followed to achieve specifications.

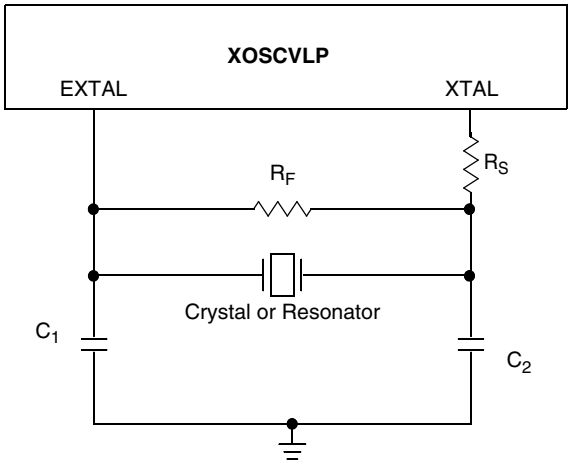


Figure 10. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

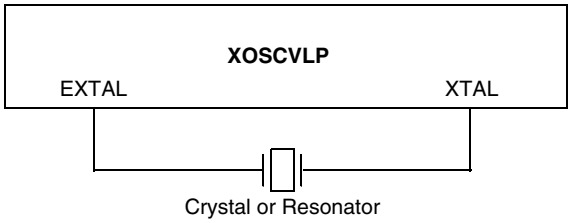


Figure 11. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 3.6 V and temperature = 25 °C	f_{int_t}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed	f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time	t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed[2] — Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
5	P	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1	f_{dco_DMX32}	—	19.92	—	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
8	C	Total deviation of DCO output from trimmed frequency[3] Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C	Δf_{dco_t}	—	–1.0 to 0.5 ±0.5	± 2 ± 1	$\%f_{dco}$
10	C	FLL acquisition time[4]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval)[5]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This parameter is characterized and not tested on each device.

4 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

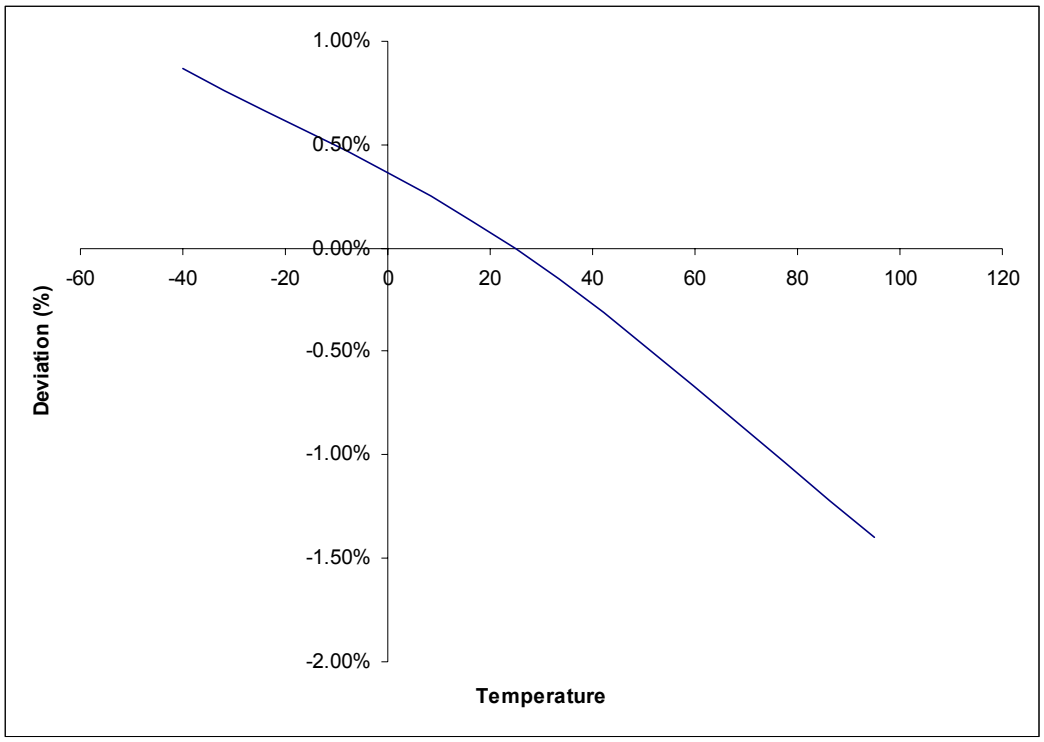


Figure 12. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 12. Control Timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	DC	—	10	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	34 x t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
9	D	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns
10	D	Voltage regulator recovery time	t_{VRR}	—	4	—	µs

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

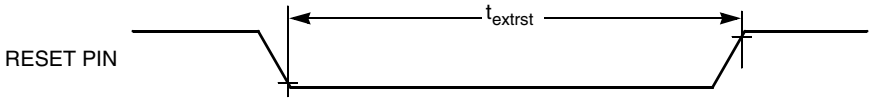


Figure 13. Reset Timing

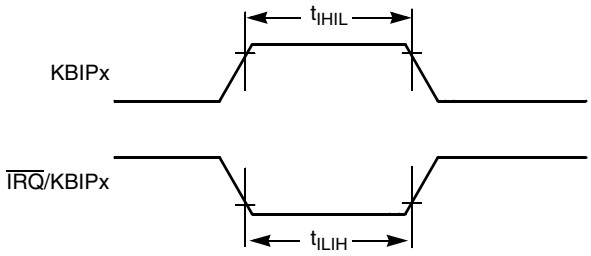


Figure 14. IRQ/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 13. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TEXT}	DC	1/4 f_{op}	MHz
2	D	External clock period	t_{TEXT}	4	—	t_{CYC}
3	D	External clock high time	t_{TCLKH}	1.5	—	t_{CYC}
4	D	External clock low time	t_{TCLKL}	1.5	—	t_{CYC}
5	D	Input capture pulse width	f_{ICPW}	1.5	—	t_{CYC}

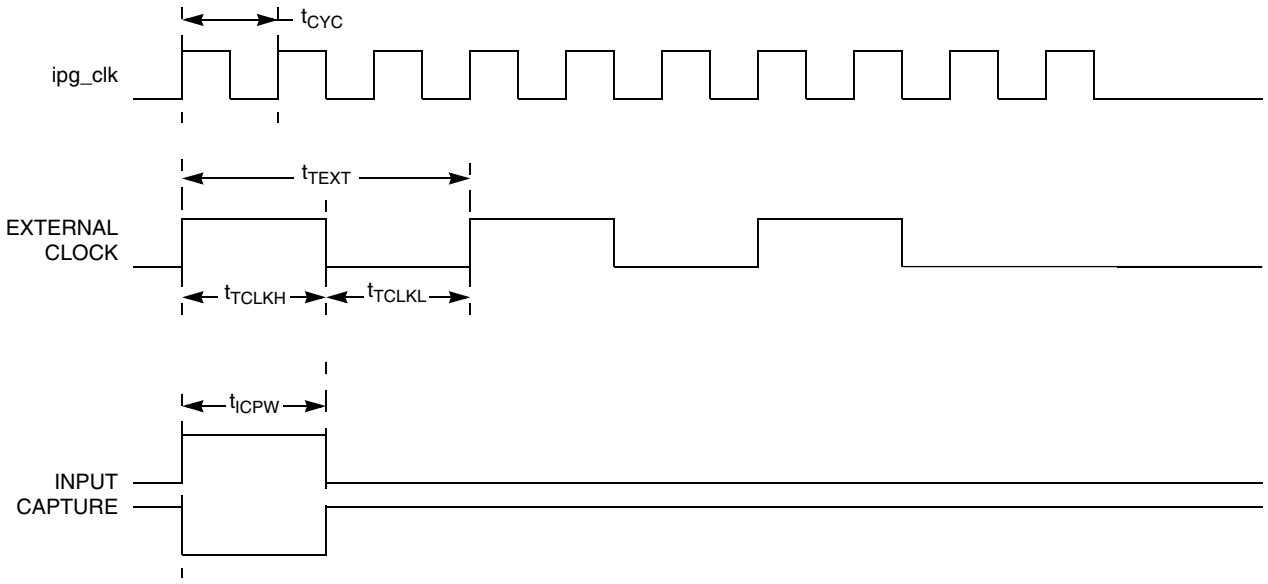


Figure 15. Timer Input Capture Pulse

3.11 Analog Comparator (ACMP) Electricals

Table 14. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{PWR}	1.8	—	3.6	V
D	Supply current (active)	I_{DDAC}	—	20	35	μA
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
P	Analog input offset voltage	V_{AIO}	—	20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

3.12 ADC Characteristics

Table 15. 12-Bit ADC Operating Conditions

Characteristic	Conditions	Symbol	Min	Typical[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V	
	Delta to V_{DD} ($V_{DD} - V_{DDA}$)[2]	ΔV_{DDA}	–100	0	100	mV	
Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)[2]	ΔV_{SSA}	–100	0	100	mV	
Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.007	0.8	μA	
Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input Resistance		R_{ADIN}	—	5	7	kΩ	
Analog Source Resistance	12 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
	8 bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low Power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

NOTE

V_{DDA}/V_{SSA} pins do not exist in 16-pin package. The signals are derived internally by double bonding to V_{DD}/V_{SS} pair of pins.

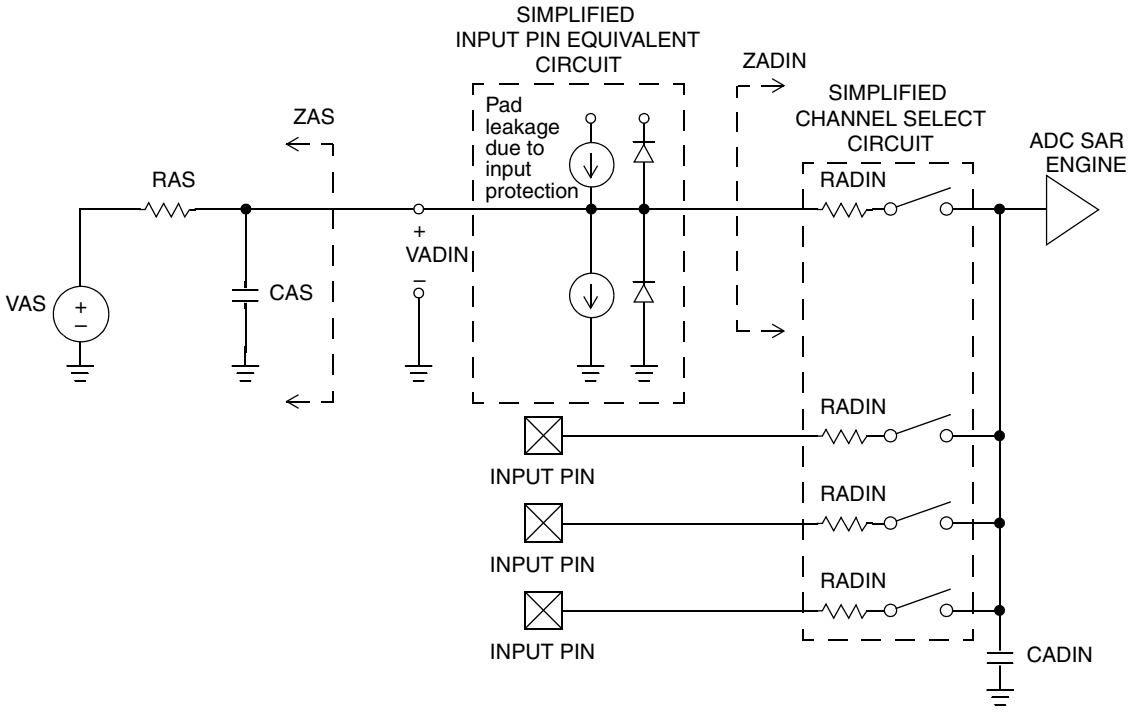


Figure 16. ADC Input Impedance Equivalency Diagram

Table 16. 12-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Characteristic	Conditions	C	Symbol	Min	Typical[1]	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	120	—	μA	
Supply Current ADLPC=1 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	202	—	μA	
Supply Current ADLPC=0 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	288	—	μA	
Supply Current ADLPC=0 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	0.532	1	mA	
Supply Current	Stop, Reset, Module Off	T	I_{DDAD}	—	0.007	0.8	μA	
ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
	Low Power (ADLPC = 1)			1.25	2	3.3		
Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
	Long Sample (ADLSMP = 1)			—	40	—		
Sample Time	Short Sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP = 1)			—	23.5	—		
Total Unadjusted Error	12-bit mode	T	E_{TUE}	—	±3.0	—	LSB[2]	For 28-pin and 24-pin packages only. Includes quantization
	10-bit mode	P		—	±1	—		
	8-bit mode	T		—	±0.5	—		
Total Unadjusted Error	10-bit mode	P	E_{TUE}	—	±1.5	—	LSB[2]	For 16-pin package only. Includes quantization
	8-bit mode	T		—	±0.7	—		
Differential Non-Linearity	12-bit mode	T	DNL	—	±1.75	—	LSB[2]	
	10-bit mode	P		—	±0.5	—		
	8-bit mode	T		—	±0.3	—		
	Monotonicity and No-Missing-Codes guaranteed							

Table 16. 12-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symbol	Min	Typical[1]	Max	Unit	Comment
Integral Non-Linearity	12-bit mode	T	INL	—	±1.5	—	LSB[2]	
	10-bit mode	C		—	±0.5	—		
	8-bit mode			—	±0.3	—		
Zero-Scale Error	12-bit mode	C	E_{ZS}	—	±1.5	—	LSB[2]	For 28-pin and 24-pin packages only. V_{ADIN} = V_{SSA}
	10-bit mode	P		—	±0.5	±1.5		
	8-bit mode	T		—	±0.5	±0.5		
Zero-Scale Error	10-bit mode	P	E_{ZS}	—	±1.5	±2.1	LSB[2]	For 16-pin package only. V_{ADIN} = V_{SSA}
	8-bit mode	T		—	±0.5	±0.7		
Full-Scale Error	12-bit mode	T	E_{FS}	—	±1	—	LSB[2]	For 28-pin and 24-pin packages only. V_{ADIN} = V_{DDA}
	10-bit mode	P		—	±0.5	±1		
	8-bit mode	T		—	±0.5	±0.5		
Full-Scale Error	10-bit mode	T	E_{FS}	—	±1	±1.5	LSB[2]	For 16-pin package only. V_{ADIN} = V_{DDA}
	8-bit mode	T		—	±0.5	±0.5		
Quantization Error	12-bit mode	D	E_Q	—	–1 to 0	—	LSB[2]	
	10-bit mode			—	—	±0.5		
	8-bit mode			—	—	±0.5		
Input Leakage Error	12-bit mode	D	E_{IL}	—	±1	—	LSB[2]	Pad leakage[3] * R_{AS}
	10-bit mode			0	±0.2	±4		
	8-bit mode			0	±0.1	±1.2		
Temp Sensor Slope	–40°C– 25°C	D	m	—	1.646	—	mV/°C	
	25°C– 85°C			—	1.769	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	701.2	—	mV	

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the memory section.

Table 17. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40°C to 85°C	$V_{prog/erase}$	1.8		3.6	V
D	Supply voltage for read operation	V_{Read}	1.8		3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
D	Byte program time (random location)[(2)]	t_{prog}	9			t_{Fcyc}
D	Byte program time (burst mode)[(2)]	t_{Burst}	4			t_{Fcyc}
D	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
D	Mass erase time[(2)]	t_{Mass}	20,000			t_{Fcyc}
D	Byte program current[3]	RI_{DDBP}	—	4	—	mA
D	Page erase current[3]	RI_{DDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40°C to + 85°C T = 25 °C	—	10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

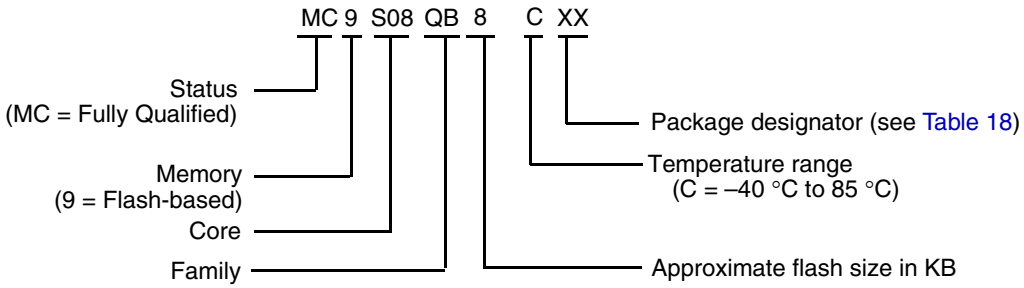
3.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

4 Ordering Information

This section contains ordering information for the device numbering system.

Example of the device numbering system:



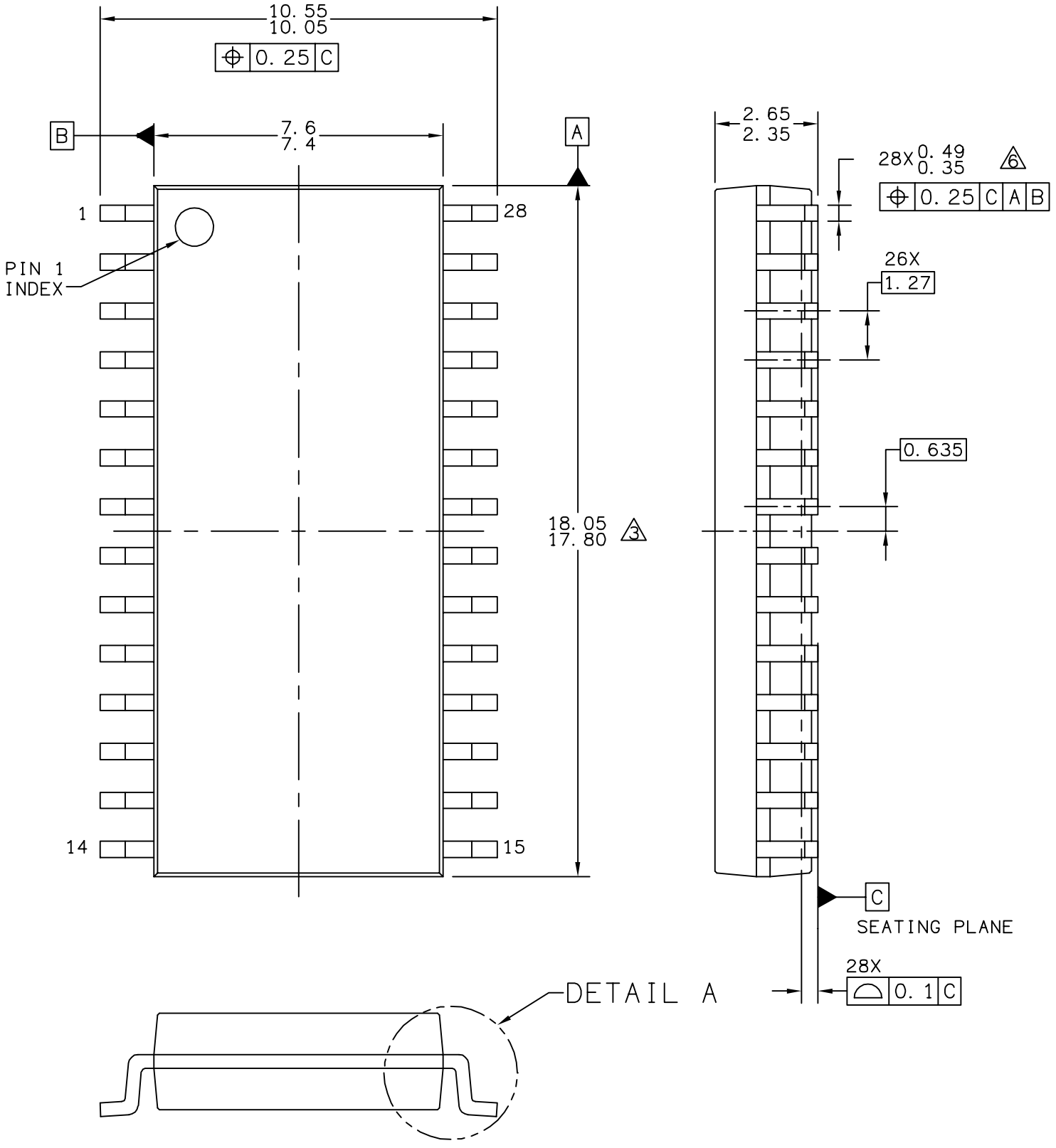
5 Package Information

Table 18. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
28	Small Outline Integrated Circuit	SOIC	WL	751F	98ASB42345B
24	Quad Flat Non-Leaded	QFN	GK	1982-01	98ARL10608D
16	Thin Shrink Small Outline Package	TSSOP	TG	948F	98ASH70247A

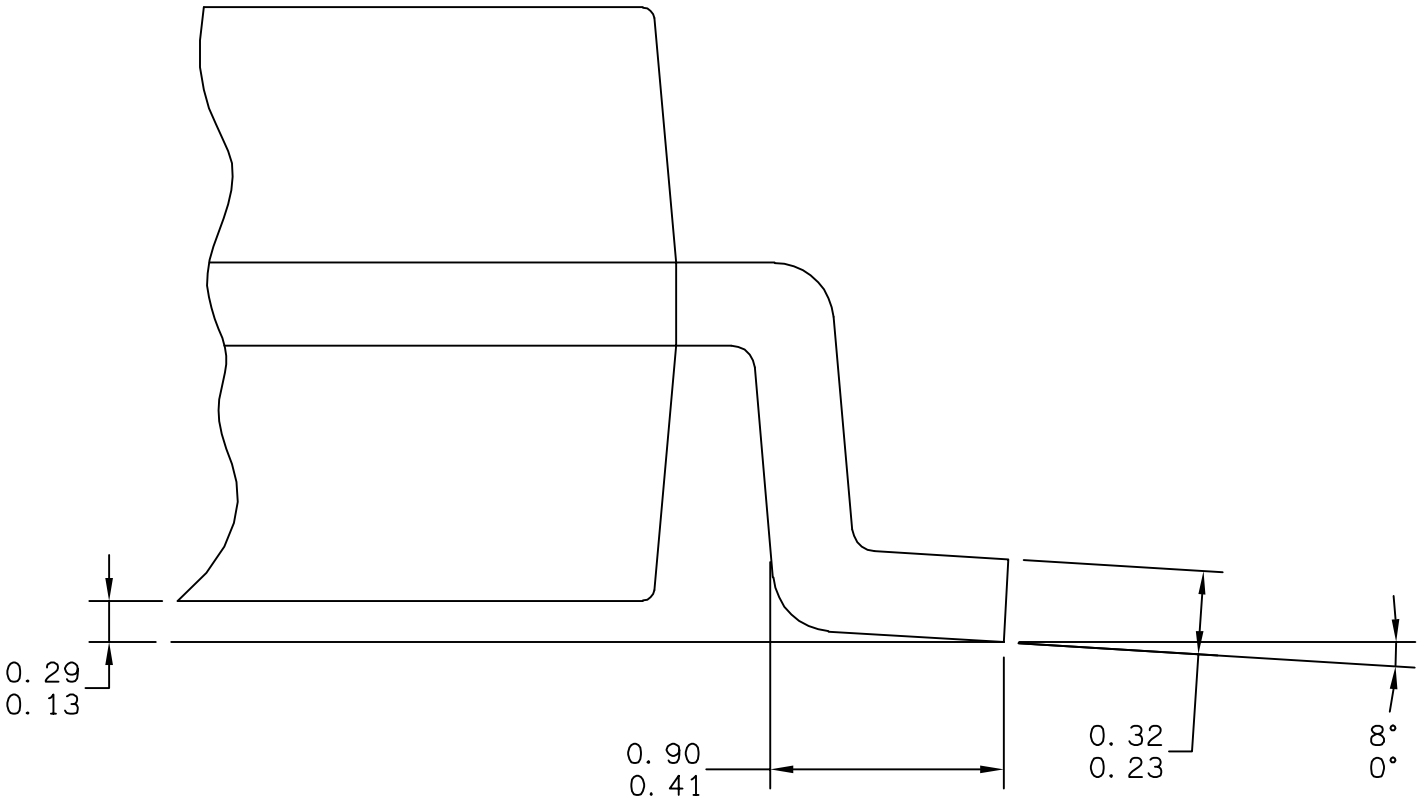
5.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 18.



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F-05	10 MAR 2005
	STANDARD: MS-013AE	



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F-05	10 MAR 2005
	STANDARD: MS-013AE	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

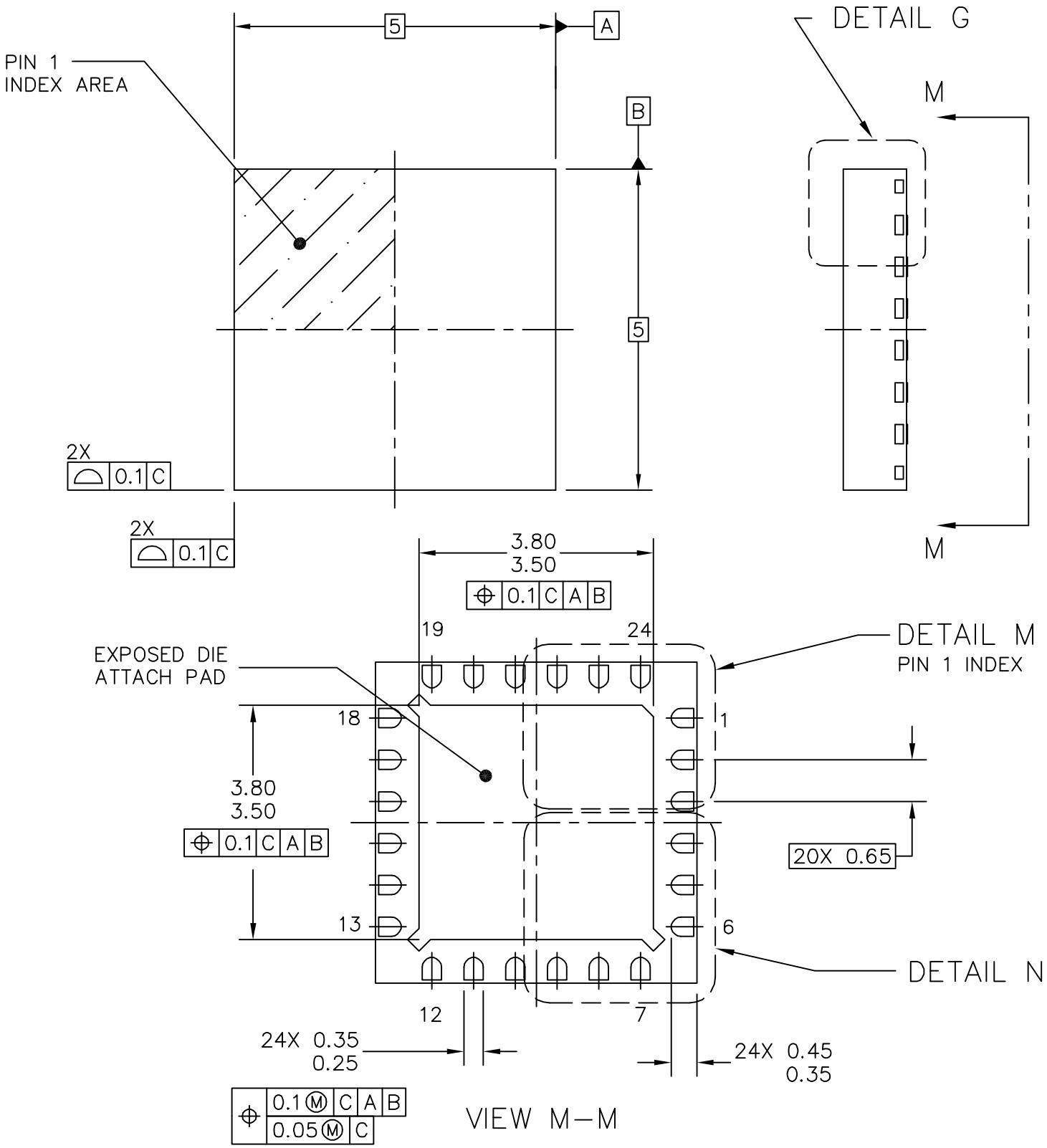
4. 751F–01 THRU –04 OBSOLETE. NEW STANDARD: 751F–05

5. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

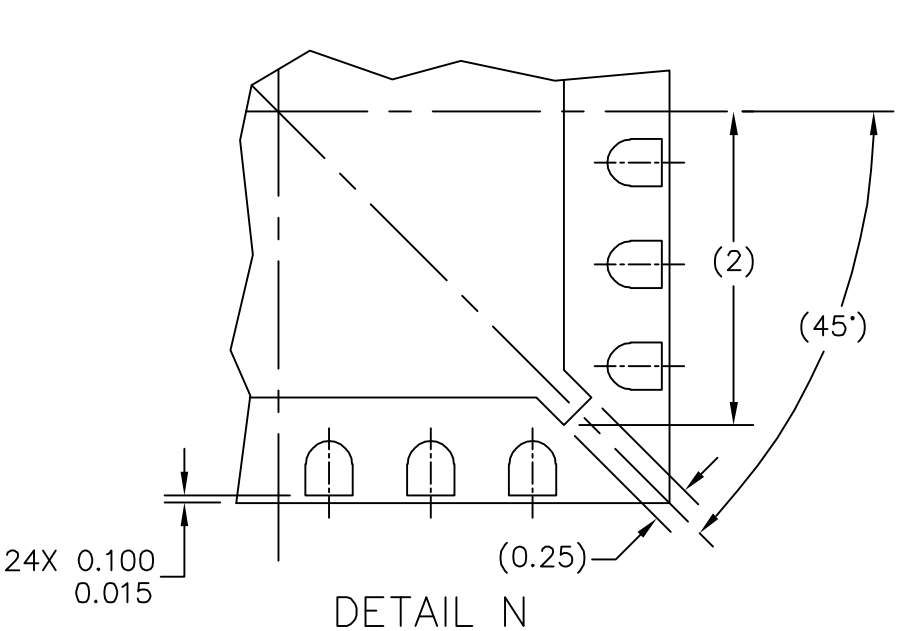
TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F–05	10 MAR 2005
	STANDARD: MS–013AE	

MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARL10608D
	PAGE: 1982
DO NOT SCALE THIS DRAWING	REV: O

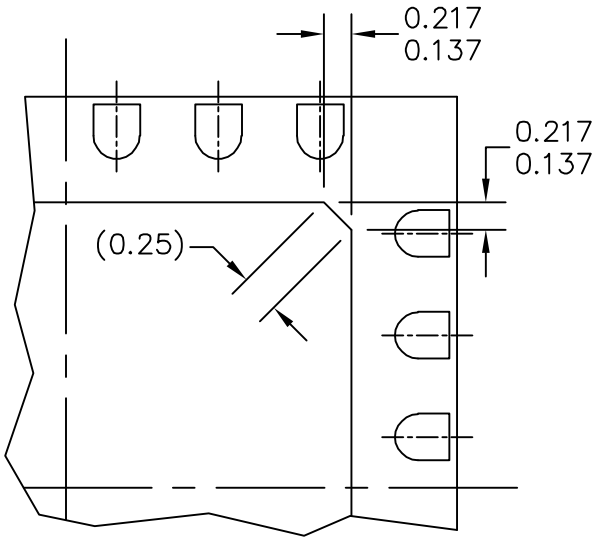


TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 24 TERMINAL, 0.65 PITCH (5 X 5 X 1)	CASE NUMBER: 1982–01	
	STANDARD: JEDEC–MO–220 VHHC–1	
	PACKAGE CODE: 6238	SHEET: 1 OF 4

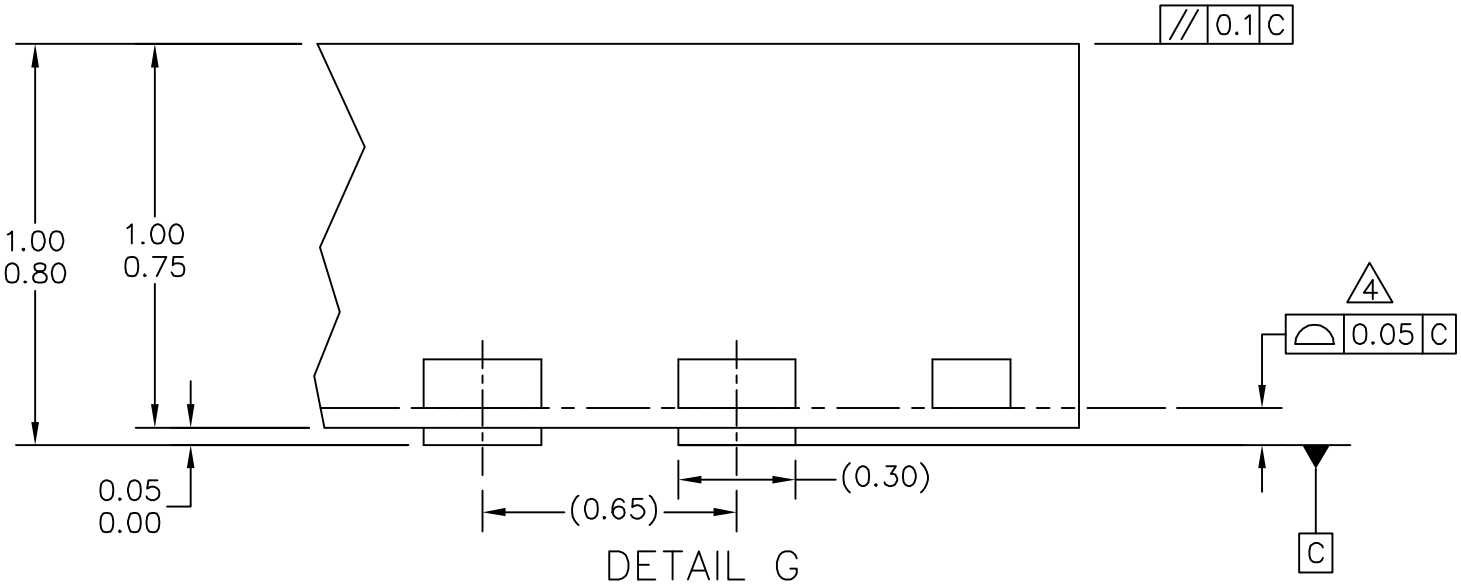
MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARL10608D
	PAGE: 1982
DO NOT SCALE THIS DRAWING	REV: O



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL M
PREFERED PIN 1 BACKSIDE IDENTIFIER



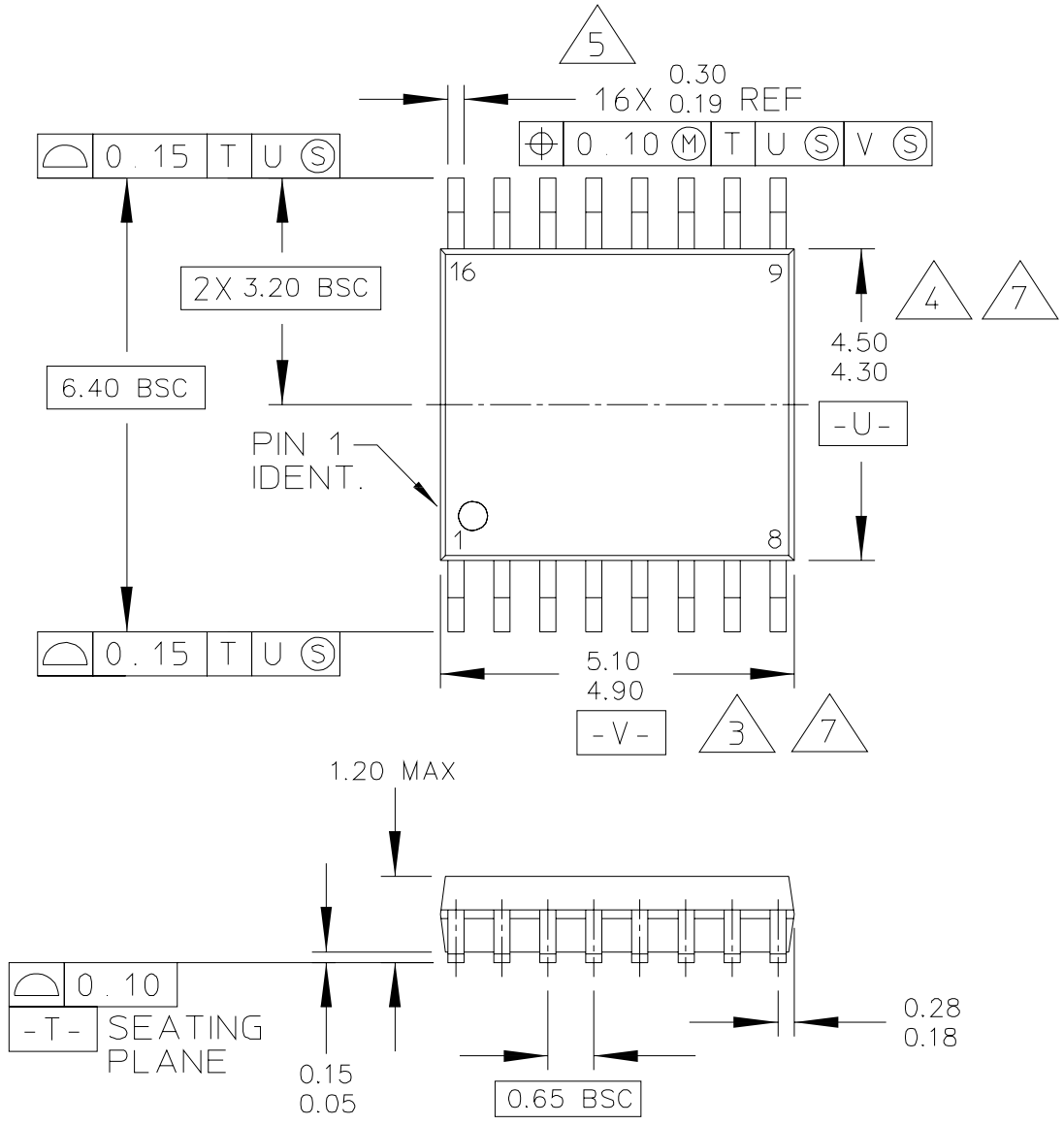
DETAIL G
VIEW ROTATED 90° CW

SEATING PLANE

TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 24 TERMINAL, 0.65 PITCH (5 X 5 X 1)	CASE NUMBER: 1982-01	
	STANDARD: JEDEC-MO-220 VHHC-1	
	PACKAGE CODE: 6238	SHEET: 2 OF 4

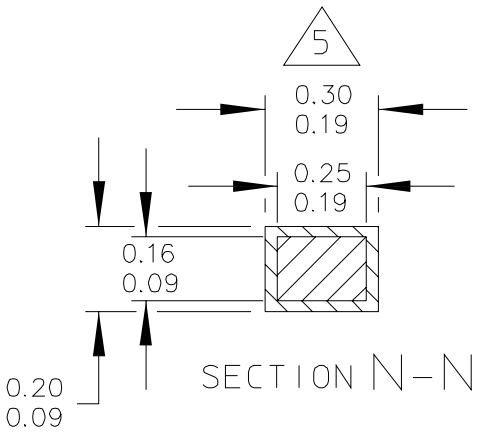
NOTES:

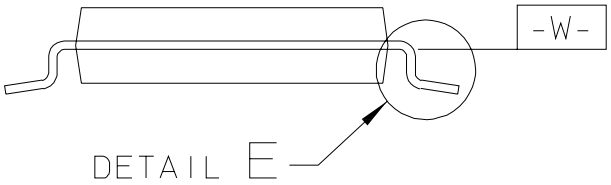
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

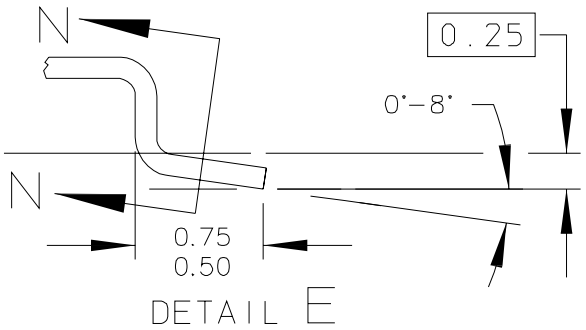


MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70247A	REV: B
16 LD TSSOP, PITCH 0.65MM	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	







	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 16 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70247A	REV: B
	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER

2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.

3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70247A	REV: B
16 LD TSSOP, PITCH 0.65MM	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	

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