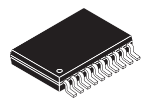
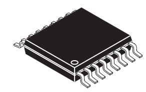
Document Number: MC9S08SF4
Rev. 4, 9/2011

MC9S08SF4

MC9S08SF4 Series



20-Pin TSSOP
Case 948E



16-Pin TSSOP
Case 948F

Features

- 8-Bit S08 Central Processor Unit (CPU)
  - Up to 40 MHz CPU at 2.7 V to 5.5 V across temperature range of –40 °C to 125 °C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - 4 KB flash read/program/erase over full operating voltage and temperature
  - 128-byte random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low power stop modes; reduced power wait mode
  - Allows clocks to remain enabled to specific peripherals in stop3 mode
- Clock Source Options
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by an internal or external reference; precision trimming of internal reference allows 0.2% resolution and 1% deviation over 0–70 °C and voltage, 2% deviation over –40–85 °C and voltage, or 3% deviation over –40–125 °C and voltage; supporting bus frequencies up to 20 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints)
  - On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes
- Peripherals
  - **IPC** — Prioritize interrupt sources besides inherent CPU interrupt table; support up to 32 interrupt sources and up to 4-level preemptive interrupt nesting
  - **ADC —** 8-channel, 10-bit resolution; 2.5 µs conversion time; automatic compare function; temperature sensor; internal bandgap reference channel; operation in stop; fully functional from 2.7 V to 5.5 V
  - **TPM** — One 40 MHz 6-channel and one 40 MHz 1-channel timer/pulse-width modulators (TPM) modules; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - **MTIM16 —** Two 16-bit modulo timers
  - **PWT** — Two 16-bit pulse width timers (PWT); selectable driving clock, positive/negative/period capture
  - **PRACMP** — Two programmable reference analog comparators with eight optional inputs for both positive and negative inputs; 32-level internal reference voltages scaled by selectable reference inputs
  - **IIC** — Inter-integrated circuit bus module capable of operation up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt-driven byte-by-byte data transfer; broadcast mode; 10-bit addressing
  - **KBI** — 4-pin keyboard interrupt module with software selectable polarity on edge or edge/level modes
  - **FDS** — Shut down output pin upon fault detection; the fault sources can be optional enabled separately; the output pin can be configured as output 1,0 and high impedance when a fault occurs based on module configuration
- Input/Output
  - 18 GPIOs including one input-only pin and one output-only pin
  - Hysteresis and configurable pullup device on all input pins; schmitt trigger on PWT input pins; configurable slew rate and drive strength on all output pins.
- Package Options
  - 16-pin TSSOP
  - 20-pin TSSOP

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

Table of Contents

Revision History

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
2	4/30/2009	Initial public release.
3	8/18/2009	Polished.
4	9/19/2011	Updated V_{AIN} in the Table 12.

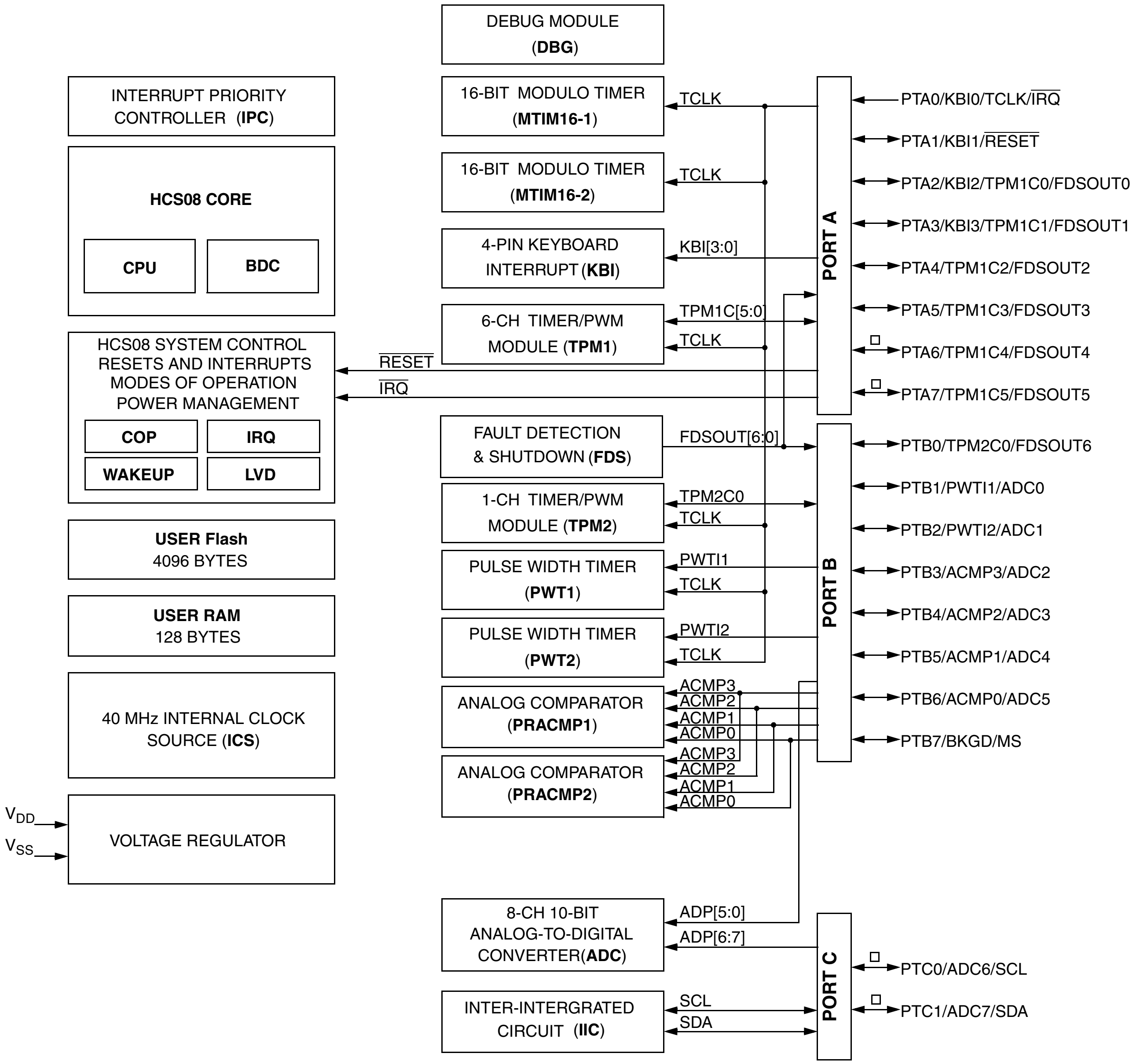
Related Documentation

Reference Manual (MC9S08SF4RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9S08SF4 MCU.



□ = Not available in the 16-pin TSSOP package

Figure 1. MC9S08SF4 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments for the MC9S08SF4 series devices.

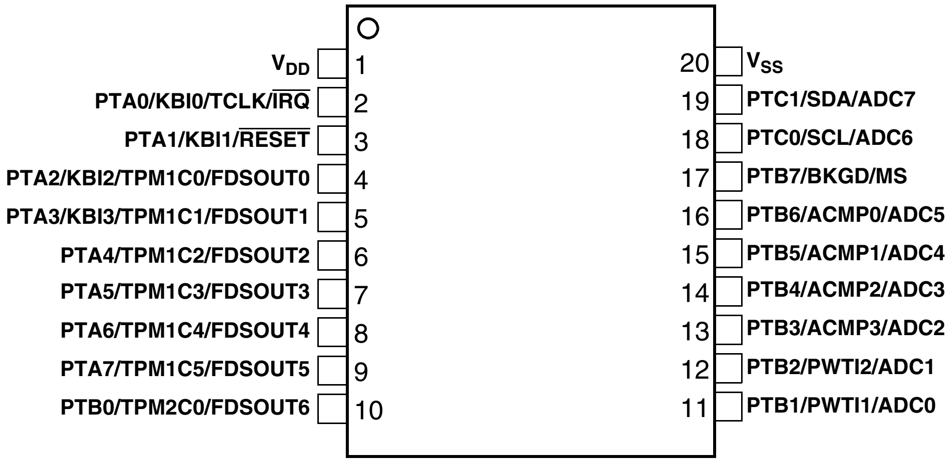


Figure 2. MC9S08SF4 in 20-Pin TSSOP Package

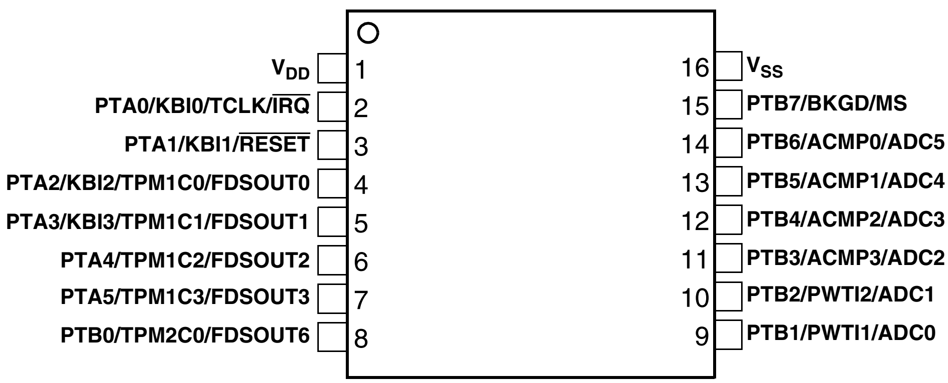


Figure 3. MC9S08SF4 in 16-Pin TSSOP Package

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08SF4 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 2 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in the external power supply going out of regulation. Ensure external V_{DD} load shunts current greater than the maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be small.

Table 3. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 125	°C
Thermal resistance (single-layer board) 20-pin TSSOP 16-pin TSSOP	θ_{JA}	 115 123	°C/W
Thermal resistance (four-layer board) 20-pin TSSOP 16-pin TSSOP	θ_{JA}	 76 75	°C/W

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

Where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

During the device qualification ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 4. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	1	
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 5. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 125 °C	I_{LAT}	±100	—	mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 6. DC Characteristics (Temperature Range = –40 to 125 °C Ambient)

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
1	P	Supply voltage (run, wait, and stop modes.)	V_{DD}	2.7	—	5.5	V
2	P	Low-voltage detection threshold — high range (V_{DD} falling) (V_{DD} rising)	V_{LVDH}	3.9 4.0	— —	4.1 4.2	V V
	P	Low-voltage detection threshold — low range (V_{DD} falling) (V_{DD} rising)	V_{LVDL}	2.48 2.54	2.56 2.62	2.64 2.7	V V
3	P	Low-voltage warning threshold — high range (V_{DD} falling) (V_{DD} rising)	V_{LVWH}	2.66 2.72	— —	2.82 2.88	V V
	P	Low-voltage warning threshold — low range (V_{DD} falling) (V_{DD} rising)	V_{LVWL}	2.84 2.90	— —	3.00 3.06	V V
4	D	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	— —	100 60	— —	mV mV
5	P	Bandgap voltage reference Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C	V_{BG}	1.185	1.200	1.215	V
6	P	Input high voltage (2.7 V ≤ V_{DD} ≤ 5.5 V) (all digital inputs)	V_{IH}	0.65 × V_{DD}	—	V_{DD} + 0.3	V

Table 6. DC Characteristics (Temperature Range = –40 to 125 °C Ambient) (continued)

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
7	P	Input low voltage (2.7 V $\leq V_{DD} \leq$ 5.5 V) (all digital inputs)	V_{IL}	$V_{SS} - 0.3$	—	$0.35 \times V_{DD}$	V
8	D	Input hysteresis (all digital inputs)	V_{hys}	$0.06 \times V_{DD}$	—	$0.30 \times V_{DD}$	V
9	P	Input Leakage Current (pins in high ohmic input mode)[1] $V_{in} = V_{DD5}$ or V_{SS5}	I_{in}	–1	—	1	μA
10	P	Internal pullup resistors[2]	R_{PU}	17.5	40.0	52.5	kΩ
	P	Internal pulldown resistor (IRQ)	R_{PD}	12.5	—	62.5	kΩ
11	C	Output high voltage All I/O pins, low-drive strength, 5 V, I_{load} = –4 mA	V_{OH}	$V_{DD} - 1.5$	—	—	V
	P	Output high voltage All I/O pins, low-drive strength, 5 V, I_{load} = –2 mA		$V_{DD} - 0.8$	—	—	V
	C	Output high voltage All I/O pins, low-drive strength, 3 V, I_{load} = –1 mA		$V_{DD} - 0.8$	—	—	V
	C	Output high voltage All I/O pins, high-drive strength, 5 V, I_{load} = –15 mA		$V_{DD} - 1.5$	—	—	V
	P	Output high voltage All I/O pins, high-drive strength, 5 V, I_{load} = –10 mA		$V_{DD} - 0.8$	—	—	V
	C	Output high voltage All I/O pins, high-drive strength, 3 V, I_{load} = –5 mA		$V_{DD} - 0.8$	—	—	V
12	C	Output low voltage All I/O pins, low-drive strength, 5 V, I_{load} = 4 mA	V_{OL}	—	—	1.5	V
	P	Output low voltage All I/O pins, low-drive strength, 5 V, I_{load} = 2 mA		—	—	0.8	V
	C	Output low voltage All I/O pins, low-drive strength, 3 V, I_{load} = 1 mA		—	—	0.8	V
	C	Output low voltage All I/O pins, high-drive strength, 5 V, I_{load} = 15 mA		—	—	1.5	V
	P	Output low voltage All I/O pins, high-drive strength, 5 V, I_{load} = 10 mA		—	—	0.8	V
	C	Output low voltage All I/O pins, high-drive strength, 3 V, I_{load} = 5 mA		—	—	0.8	V
13	D	Maximum total I_{OH} for all port pins 5 V 3 V	$\|I_{OHT}\|$	— —	— —	100 60	mA
	D	Maximum total I_{OL} for all port pins 5 V 3 V	$\|I_{OLT}\|$	— —	— —	100 60	mA
14	D	dc injection current[2, 3, 4, 5] $V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$ Single pin limit Total MCU limit, includes sum of all stressed pins	$\|I_{IC}\|$	— —	— —	0.2 5	mA mA
15	D	Input capacitance (all non-supply pins)	C_{In}	—	—	7	pF

[1] Maximum leakage current occurs at a maximum operating temperature. The current decreases by approximately one-half for each 8 °C to 12 °C in the temperature range from 50 °C to 125 °C.

[2] Measurement condition for pull resistors: $V_{In} = V_{SS}$ for pullup and $V_{In} = V_{DD}$ for pulldown.

[3] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[4] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

[5] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which reduces overall power consumption).

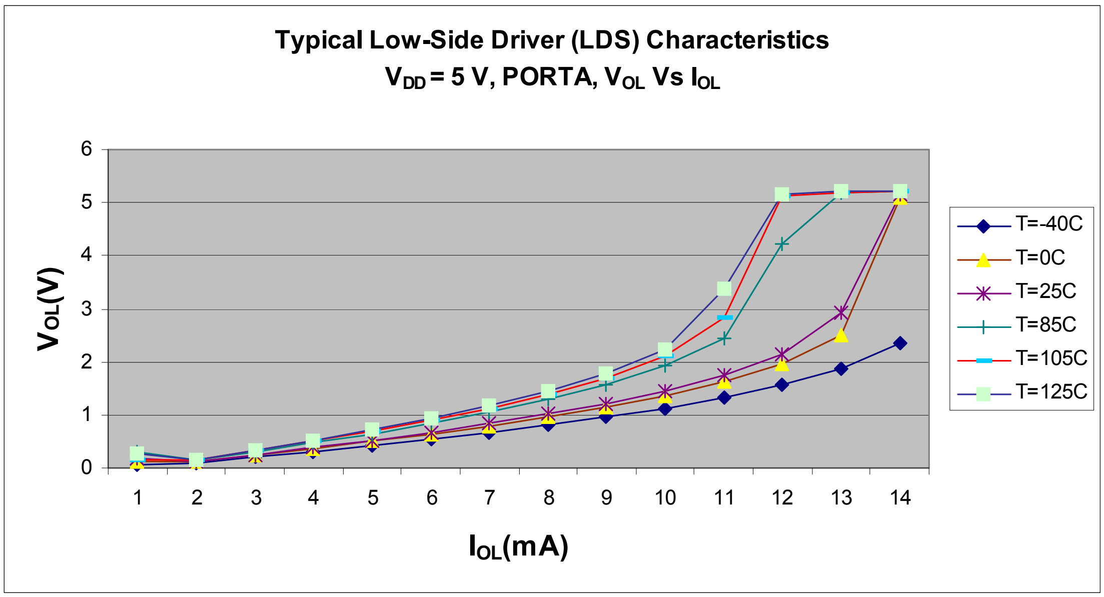


Figure 4. Typical Low-Side Driver (Sink) Characteristics
Low Drive (PTxDSn = 0), V_{DD} = 5.0 V, V_{OL} vs. I_{OL}

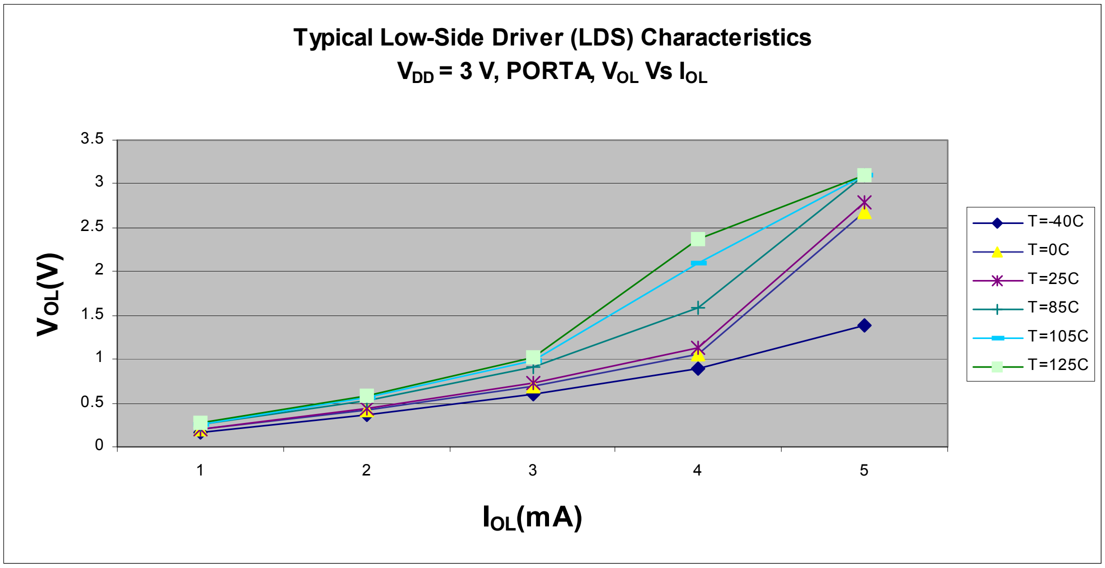


Figure 5. Typical Low-Side Driver (Sink) Characteristics
Low Drive (PTxDSn = 0), V_{DD} = 3.0 V, V_{OL} vs. I_{OL}

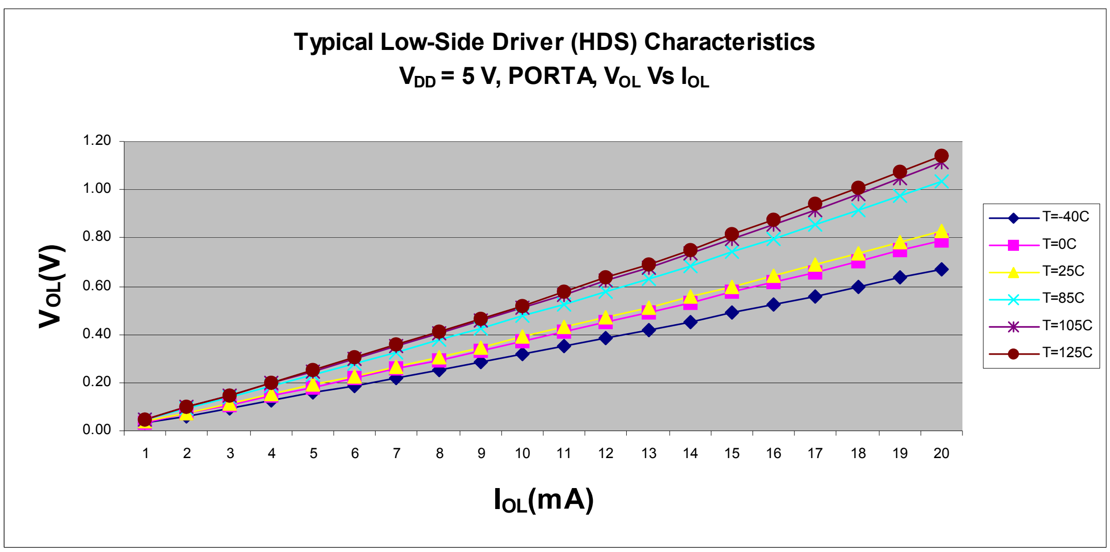


Figure 6. Typical Low-Side Driver (Sink) Characteristics
High Drive (PTxDSn = 1), V_{DD} = 5.0 V, V_{OL} vs. I_{OL}

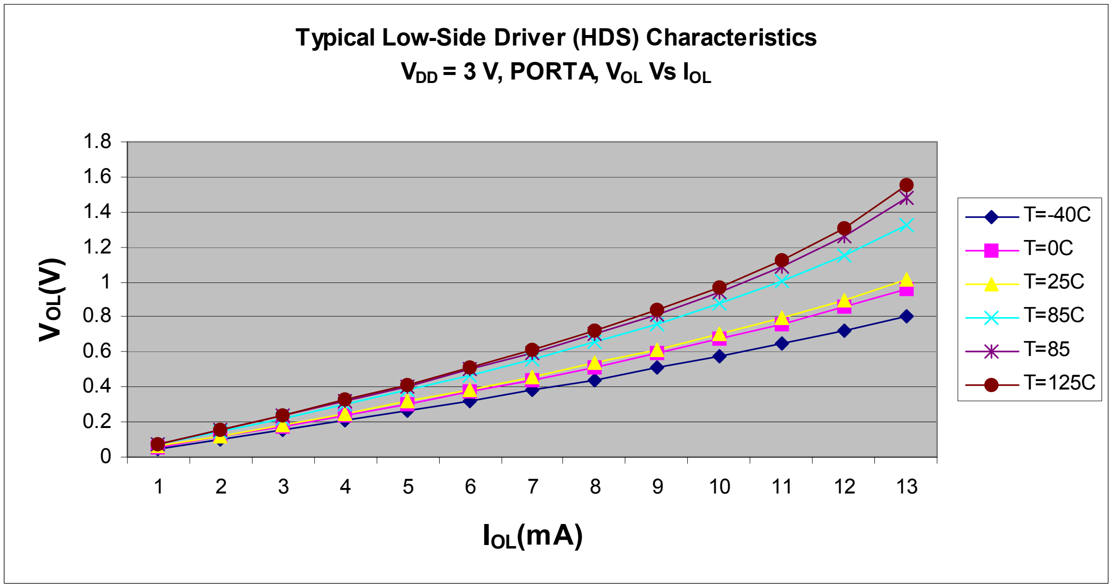


Figure 7. Typical Low-Side Driver (Sink) Characteristics High Drive (PTxDSn = 1), V_{DD} = 3.0 V, V_{OL} vs. I_{OL}

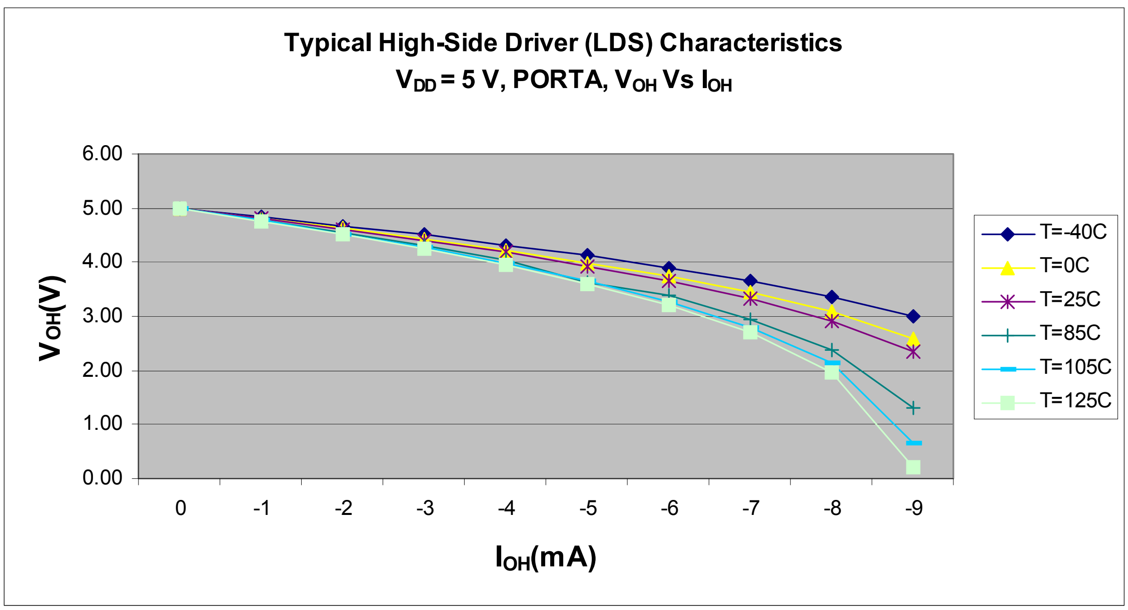


Figure 8. Typical High-Side Driver (Source) Characteristics Low Drive (PTxDSn = 0), V_{DD} = 5.0 V, V_{OH} vs. I_{OH}

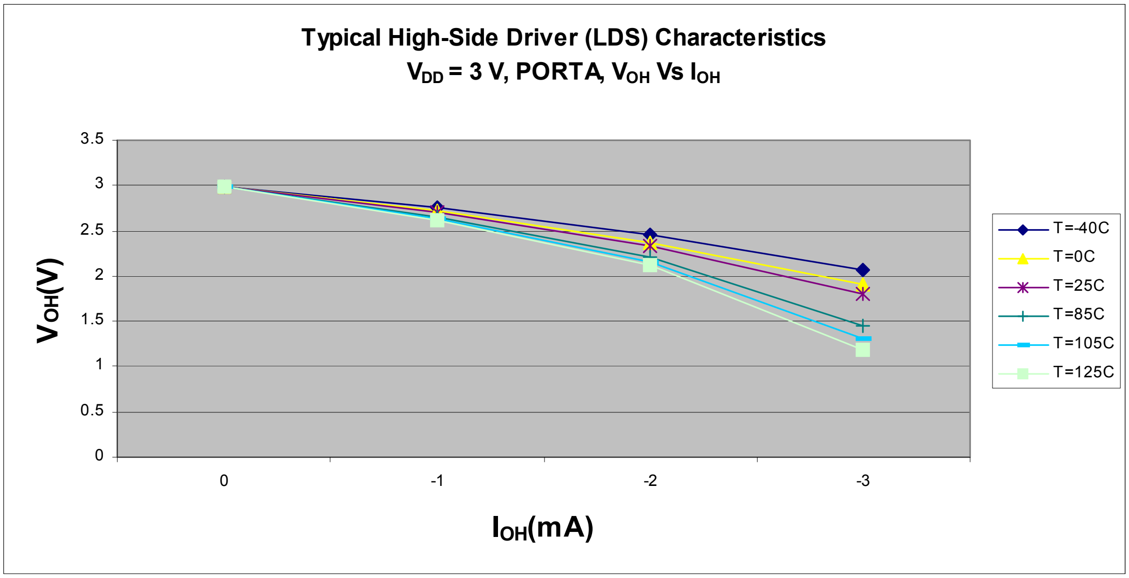


Figure 9. Typical High-Side Driver (Source) Characteristics Low Drive (PTxDSn = 0), V_{DD} = 3.0 V, V_{OH} vs. I_{OH}

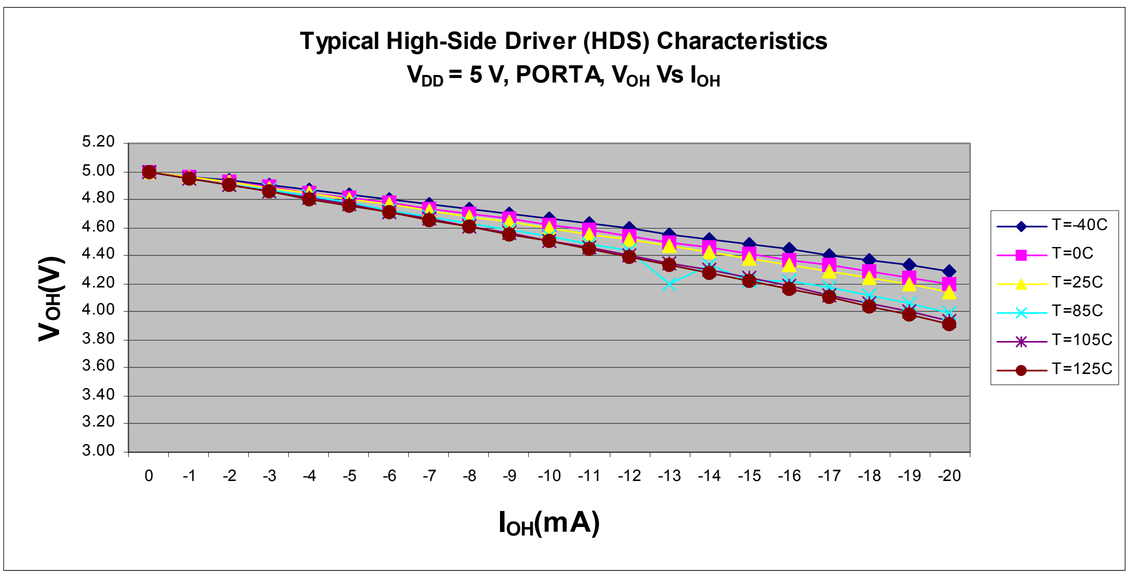


Figure 10. Typical High-Side Driver (Source) Characteristics High Drive (PTxDSn = 1), V_{DD} = 5.0 V, V_{OH} vs. I_{OH}

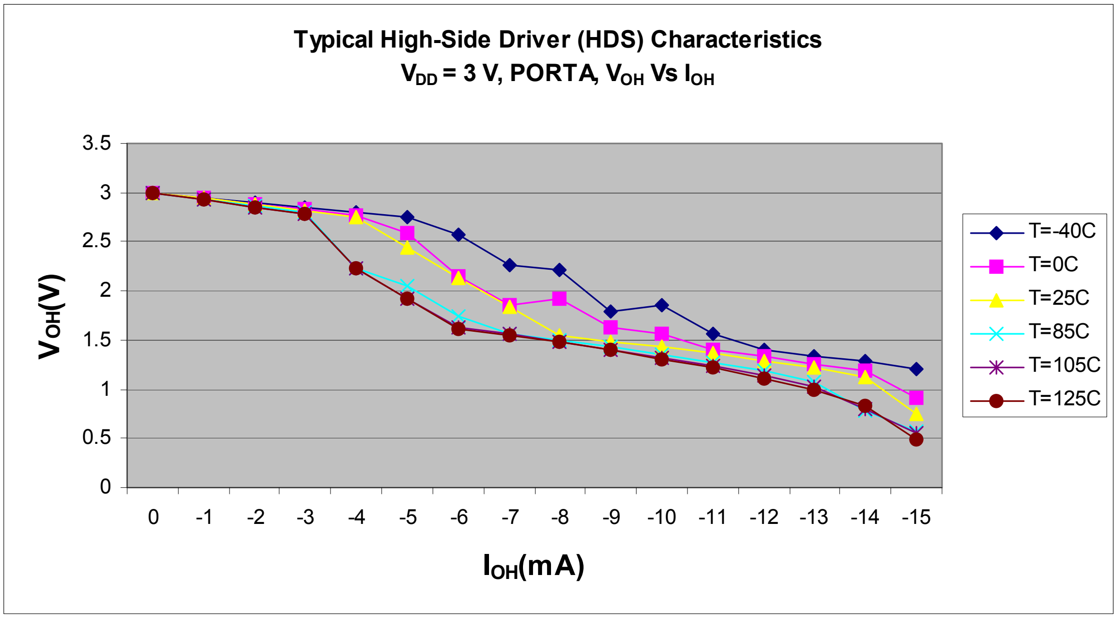


Figure 11. Typical High-Side Driver (Source) Characteristics
High Drive (PTxDSn = 1), V_{DD} = 3.0 V, V_{OH} vs. I_{OH}

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 7. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	P	Run supply current[3] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	RI_{DD}	5	1.75	1.77	mA
	D			3	1.71	1.73	
2	P	Run supply current[3] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)	RI_{DD}	5	5.69	6.25	mA
	D			3	4.63	4.66	
3	P	Run mode supply current[3] measured at (CPU clock = 40 MHz, f_{Bus} = 20 MHz)	RI_{DD}	5	11.53	12.00	mA
	D			3	10.39	11.00	
4	P	Wait mode supply current[4] measured at (f_{Bus} = 8 MHz)	WI_{DD}	5	3.95	4.54	mA
	D			3	3.58	4.00	
5	P	Wait mode supply current[4] measured at (f_{Bus} = 20 MHz)	WI_{DD}	5	8.36	9.62	mA
	D			3	7.97	8.07	
6	P	Stop2 mode supply current –40 to 85 °C	$S2I_{DD}$	5	1.99	18.47	µA
	P	–40 to 125 °C				100	
	D	–40 to 85°C		3	1.95	16.9	
	D	–40 to 125°C				90	

Table 7. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
7	P	Stop3 mode supply current –40 to 85 °C	$S3I_{DD}$	5	2	18.4	μA
	P	–40 to 125 °C				100	
	D	–40 to 85 °C		3	1.97	16.82	
	D	–40 to 125 °C				90	
8	D	PRACMP (PRG disabled) adder to stop3, 25 °C	—	5	28.87	—	nA
	D			3	27.06	—	nA
9	D	PRACMP (PRG enabled) adder to stop3, 25 °C	—	5	79.42	—	nA
	D			3	57.4	—	nA
10	D	ADC adder to stop2 or stop3, 25 °C	—	5	25	—	nA
	D			3	6	—	nA
11	D	LVD adder to stop3 (LVDE = LVDSE = 1)	—	5	83.52	—	nA
	D			3	83.52	—	nA
12	D	Adder to stop3 for oscillator enabled (IREFSTEN = 1)	—	5	0.03	—	μA
	D			3	0.01	—	μA
13	D	TPM1 and TPM2 adder to run mode, 25 °C (CPU clock = 40 MHz, f_{Bus} = 20 MHz)	—	5	0.16	—	mA
	D			3	0.18	—	mA
14	D	PWT1 and PWT2 adder to run mode, 25 °C (CPU clock = 40 MHz, f_{Bus} = 20 MHz)	—	5	0.43	—	mA
	D			3	0.41	—	mA
15	D	PRACMP adder to run mode, 25 °C (CPU clock = 40 MHz, f_{Bus} = 20 MHz)	—	5	0.35	—	mA
	D			3	0.35	—	mA
16	D	MTIM1 and MTIM2 adder to run mode, 25 °C (CPU clock = 40 MHz, f_{Bus} = 20 MHz)	—	5	0.26	—	mA
	D			3	0.24	—	mA
17	D	ADC adder to run mode, 25 °C (CPU clock = 40 MHz, f_{Bus} = 20 MHz)	—	5	0.42	—	mA
	D			3	0.32	—	mA
18	D	IIC adder to run mode, 25 °C (CPU clock = 40 MHz, f_{Bus} = 20 MHz)	—	5	0.56	—	mA
	D			3	0.53	—	mA

[1] Typicals are measured at 25 °C.

[2] Values given here are preliminary estimates prior to completing characterization.

[3] All modules except ADC active, and does not include any dc loads on port pins.

[4] Most customers are expected to find that the auto-wakeup from a stop mode can be used instead of the higher current wait mode.

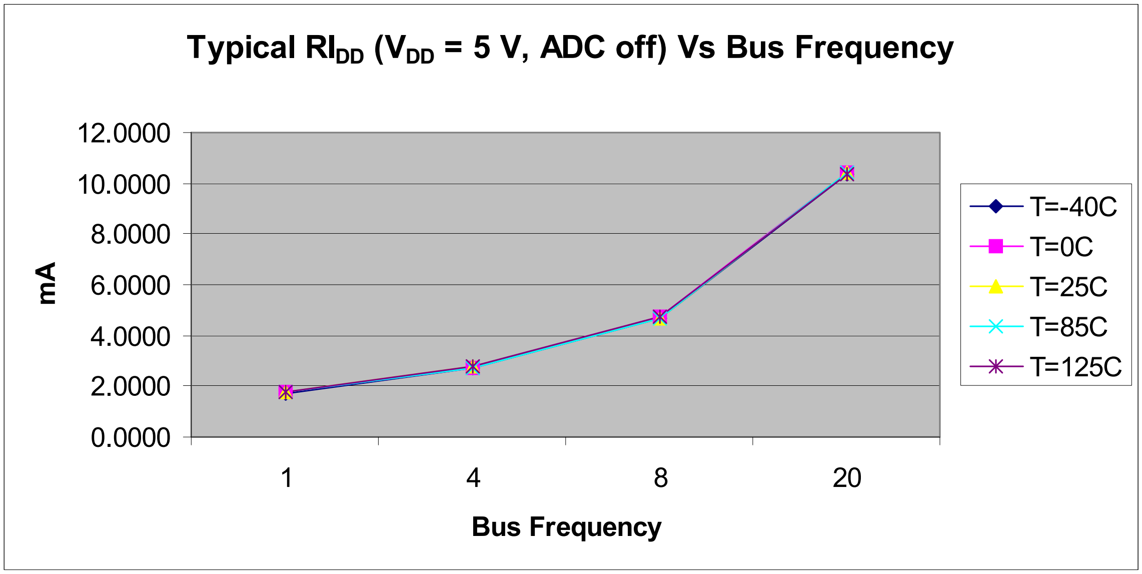


Figure 12. Typical Run I_{DD} vs. Bus Freq. (FEI) (ADC off)

3.8 ICS Characteristics

Refer to Figure 13 for crystal or resonator circuits.

Table 8. ICS Specifications (Temperature Range = –40 to 125 °C Ambient)

<table>
<tr><th>No.</th><th>C</th><th colspan="2">Characteristic</th><th>Symbol</th><th>Minimum</th><th>Typical[1]</th><th>Maximum</th><th>Unit</th></tr>
<tr><td>1</td><td>T</td><td colspan="2">Internal reference start-up time</td><td>t_{IRST}</td><td>—</td><td>60</td><td>100</td><td>µs</td></tr>
<tr><td>2</td><td>P</td><td colspan="2">Average internal reference frequency — trimmed</td><td>f_{int_t}</td><td>—</td><td>39.0625</td><td>—</td><td>kHz</td></tr>
<tr><td rowspan="2">3</td><td>P</td><td rowspan="2">DCO output frequency range — trimmed</td><td>Low range (DRS = 00)</td><td rowspan="2">f_{dco_t}</td><td>16</td><td>—</td><td>20</td><td rowspan="2">MHz</td></tr>
<tr><td>P</td><td>Middle range (DRS = 10)</td><td>32</td><td>—</td><td>40</td></tr>
<tr><td>4</td><td>P</td><td colspan="2">Total deviation of DCO output from trimmed frequency[2]
Over full voltage and temperature range of –40 °C to 125 °C</td><td rowspan="3">Δf_{dco_t}</td><td rowspan="3">—</td><td>–1.0 to 0.5</td><td>±3</td><td rowspan="3">$\%f_{dco}$</td></tr>
<tr><td>5</td><td>D</td><td colspan="2">Total deviation of DCO output from trimmed frequency
Over full voltage and temperature range of –40 °C to 85 °C</td><td>–1.0 to 0.5</td><td>±2</td></tr>
<tr><td>6</td><td>D</td><td colspan="2">Total deviation of DCO output from trimmed frequency
Over fixed voltage and temperature range of 0 to 70 °C</td><td>±0.5</td><td>±1</td></tr>
<tr><td>7</td><td>C</td><td colspan="2">FLL acquisition time[2,3]</td><td>$t_{Acquire}$</td><td>—</td><td>—</td><td>1</td><td>ms</td></tr>
<tr><td>8</td><td>C</td><td colspan="2">Long term jitter of DCO output clock (averaged over a 2 ms interval) [4]</td><td>C_{Jitter}</td><td>—</td><td>0.02</td><td>0.2</td><td>$\%f_{dco}$</td></tr>
</table>

[1] Data in the Typical column was characterized at 5.0 V, 25 °C, or the typical recommended value.

[2] This parameter is characterized and not tested on each device.

[3] This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, DMX32 bit changed, DRS bit changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, and FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

[4] Jitter is the average deviation from the programmed frequency measured over the specified interval at the maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and a variation in the crystal oscillator frequency increases the C_{Jitter} percentage for a given interval.

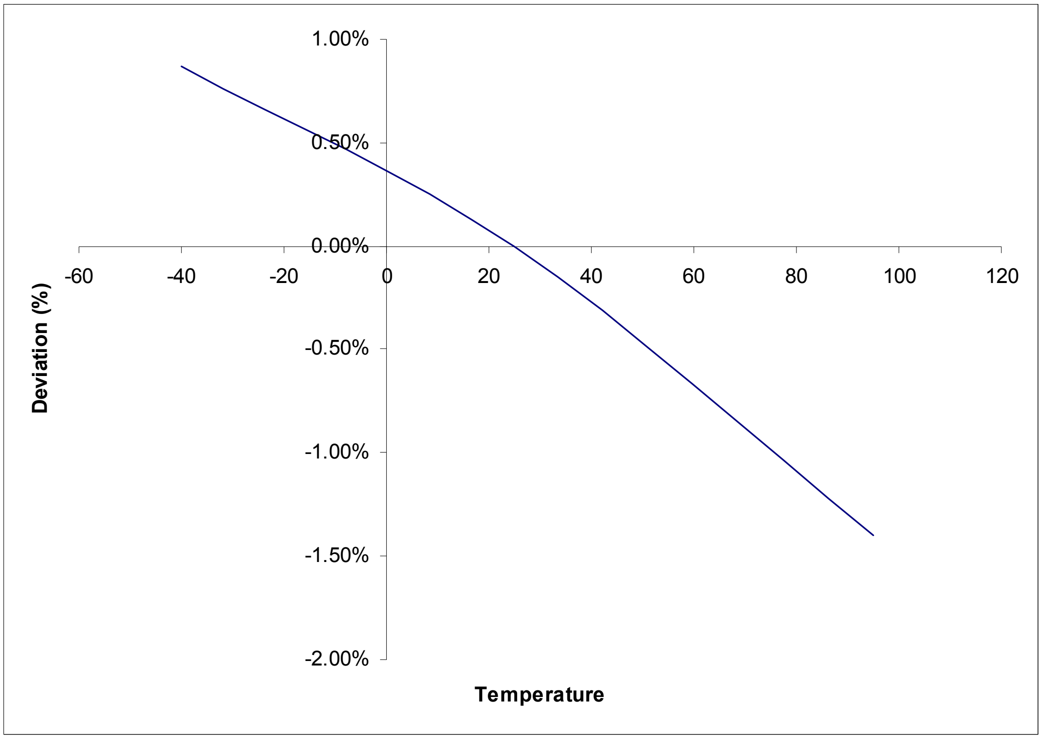


Figure 13. Deviation of DCO Output from Trimmed Frequency (20 MHz, 5.0 V)

3.9 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.9.1 Control Timing

Table 9. Control Timing

Parameter	Symbol	Minimum	Typical[1]	Maximum	Unit
Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	1	—	20	MHz
External reset pulse width[2]	t_{extrst}	100	—	—	ns
IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 1.5 t_{cyc}	—	—	ns
KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 1.5 t_{cyc}	—	—	ns
Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	3 30	— —	ns
BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [5]	t_{MSH}	100	—	—	μs

1 Data in Typical column was characterized at 5.0 V, 25 °C.

2 This is the shortest pulse that is guaranteed to be recognized.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 125 °C.

5 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

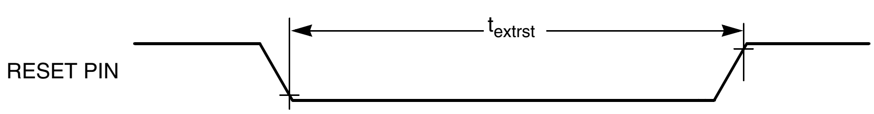


Figure 14. Reset Timing

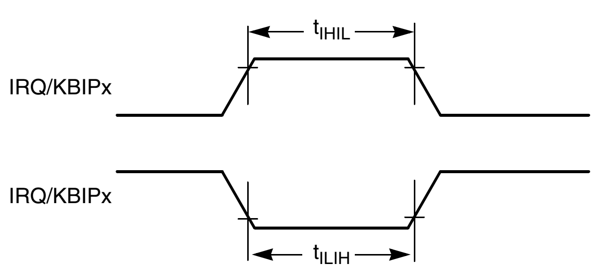


Figure 15. IRQ/KBIPx Timing

3.9.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 10. TPM/MTIM Input Timing

Function	Symbol	Min	Max	Unit
External clock frequency	f_{TCLK}	dc	$f_{timer}/4$	MHz
External clock period	t_{TCLK}	4	—	t_{cyc}
External clock high time	t_{clkh}	1.5	—	t_{cyc}
External clock low time	t_{clkl}	1.5	—	t_{cyc}
Input capture pulse width for TPM	t_{ICPW}	1.5	—	t_{cyc}
Timer clock frequency	f_{timer}	—	40	MHz

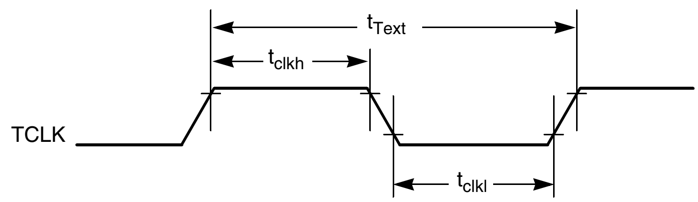


Figure 16. Timer External Clock

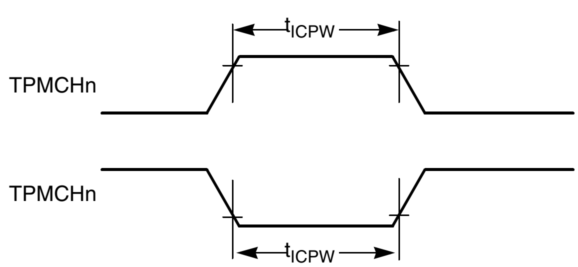


Figure 17. Timer Input Capture Pulse

3.10 ADC Characteristics

Table 11. ADC Characteristics

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	D	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1	$V_{DDA} \le 3.6$ V (3.0 V Typ)	I_{DDA}	—	110	—	µA	Over temperature (Typ 25°C)
	D		$V_{DDA} \le 5.5$ V (5.0 V Typ)		—	130	—		
2	D	Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1	$V_{DDA} \le 3.6$ V (3.0 V Typ)	I_{DDA}	—	200	—	µA	
	D		$V_{DDA} \le 5.5$ V (5.0 V Typ)		—	220	—		
3	D	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1	$V_{DDA} \le 3.6$ V (3.0 V Typ)	I_{DDA}	—	320	—	µA	
	D		$V_{DDA} \le 5.5$ V (5.0 V Typ)		—	360	—		
4	D	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1	$V_{DDA} \le 3.6$V (3.0 V Typ)	I_{DDA}	—	580	—	µA	
	D		$V_{DDA} \le 5.5$V (5.0 V Typ)		—	660	—		
5	D	Supply current	Stop, Reset, Module Off	I_{DDA}	—	<1	100	nA	
6	D	Ref voltage high	—	V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	
	D	Ref coltage low	—	V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
7	D	ADC conversion clock	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	$t_{ADCK} = 1/f_{ADCK}$
	D		Low power (ADLPC = 1)		0.4	—	4.0		
8	D	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2.5	4	6.6	MHz	$t_{ADACK} = 1/f_{ADACK}$
	D		Low power (ADLPC = 1)		1.25	2	3.3		
9	D	Conversion time	Short sample (ADLSMP = 0)	t_{ADC}	20	20	23	t_{ADCK} cycles	Add 2 to 5 $t_{Bus} = 1/f_{Bus}$ cycles
	D		Long sample (ADLSMP = 1)		40	40	43		
10	D	Sample time	Short sample (ADLSMP = 0)	t_{ADS}	4	4	4	t_{ADCK} cycles	
	D		Long sample (ADLSMP = 1)		24	24	24		
11	D	Input voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
12	D	Input capacitance	—	C_{ADIN}	—	7	10	pF	Not Tested
13	D	Input impedance	—	R_{ADIN}	—	5	15	kΩ	Not Tested
14	D	Analog source impedance	—	R_{AS}	—	—	10^2	kΩ	External to MCU

Table 11. ADC Characteristics (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
15	D	Ideal resolution (1LSB)	10-bit mode	RES	2.637	4.883	5.371	mV	$V_{REFH}/2^N$
	D		8-bit mode		10.547	19.53	21.48		
16	D	Total unadjusted error	10-bit mode	E_{TUE}	0	±1.5	±3.5	LSB	Includes quantization
	D		8-bit mode		0	±0.7	±1.0		
17	P	Differential non-linearity[3]	10-bit mode	DNL	0	±0.5	±1.0	LSB	
	C		8-bit mode		0	±0.3	±0.5		
18	P	Integral non-linearity	10-bit mode	INL	0	±0.5	±1.0	LSB	
	C		8-bit mode		0	±0.3	±0.5		
19	D	Zero-scale error	10-bit mode	E_{ZS}	0	±1.5	±3.1	LSB	$V_{ADIN} = V_{SSA}$
	D		8-bit mode		0	±0.5	±0.7		
20	D	Full-scale error	10-bit mode	E_{FS}	0	±1.0	±1.5	LSB	$V_{ADIN} = V_{DDA}$
	D		8-bit mode		0	±0.5	±0.5		
21	D	Quantization error	10-bit mode	E_Q	—	—	±0.5	LSB	8-bit mode is not truncated
22	P	Temp sensor slope	–40–25 °C	—	—	3.266	—	—	
			25–125 °C	—	—	3.638	—	—	
23	P	Temp sensor voltage	—	—	—	1.396	—	—	

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2 At 4 MHz, for maximum frequency, use proportionally lower source impedance.
3 Monotonicity and no-missing-codes guaranteed

3.11 PRACMP Characteristics

Table 12. PRACMP Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	P	Supply voltage	V_{PWR}	2.70	—	5.50	V
2	C	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	60	µA
3	C	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	µA
4	C	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA
5	C	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
6	C	Analog input offset voltage	V_{AIO}	—	5	40	mV
7	C	Analog comparator hysteresis	V_H	3.0	—	20.0	mV
8	C	Analog input leakage current	I_{ALKG}	—	—	1	nA
9	C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs

Table 12. PRACMP Specifications (continued)

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
10	D	Programmable reference generator inputs	V_{In1} (V_{DD50})	2.7	5.0	5.5	V
11	D	Programmable reference generator inputs	V_{In2} (V_{DD25})	2.25	2.5	2.75	V
12	C	Programmable reference generator step size	V_{step}	–0.25	0	0.25	LSB
13	P	Programmable reference generator voltage range	V_{prgout}	$V_{In}/32$	—	V_{in}	V

3.12 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 13. Flash Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage for program/erase –40°C to 125°C	$V_{prog/erase}$	2.7	—	5.5	V
Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
Byte program time (random location)[(2)]	t_{prog}		9		t_{Fcyc}
Byte program time (burst mode)[(2)]	t_{Burst}		4		t_{Fcyc}
Page erase time[2]	t_{Page}		4000		t_{Fcyc}
Mass erase time[(2)]	t_{Mass}		20,000		t_{Fcyc}
Program/erase endurance[3] T_L to T_H = –40 °C to 125 °C T = 25°C		 10,000 —	 — 100,000	 — —	cycles
Data retention[4]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

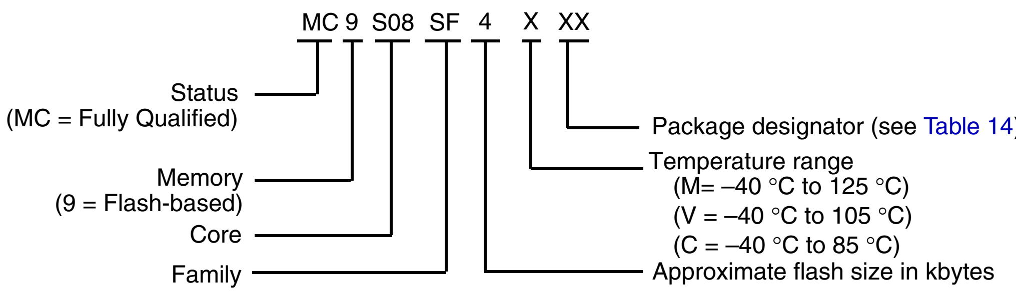
3 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Delta defines typical endurance, please refer to engineering bulletin *Typical Endurance for Nonvolatile Memory* (document EB619/D).

4 **Typical data retention** values are based on intrinsic capability of the technology measured at a high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Delta defines typical data retention, please refer to engineering bulletin *Typical Data Retention for Nonvolatile Memory* (document EB618/D).

4 Ordering Information

This section contains ordering information for the device numbering system.

Example of the device numbering system:



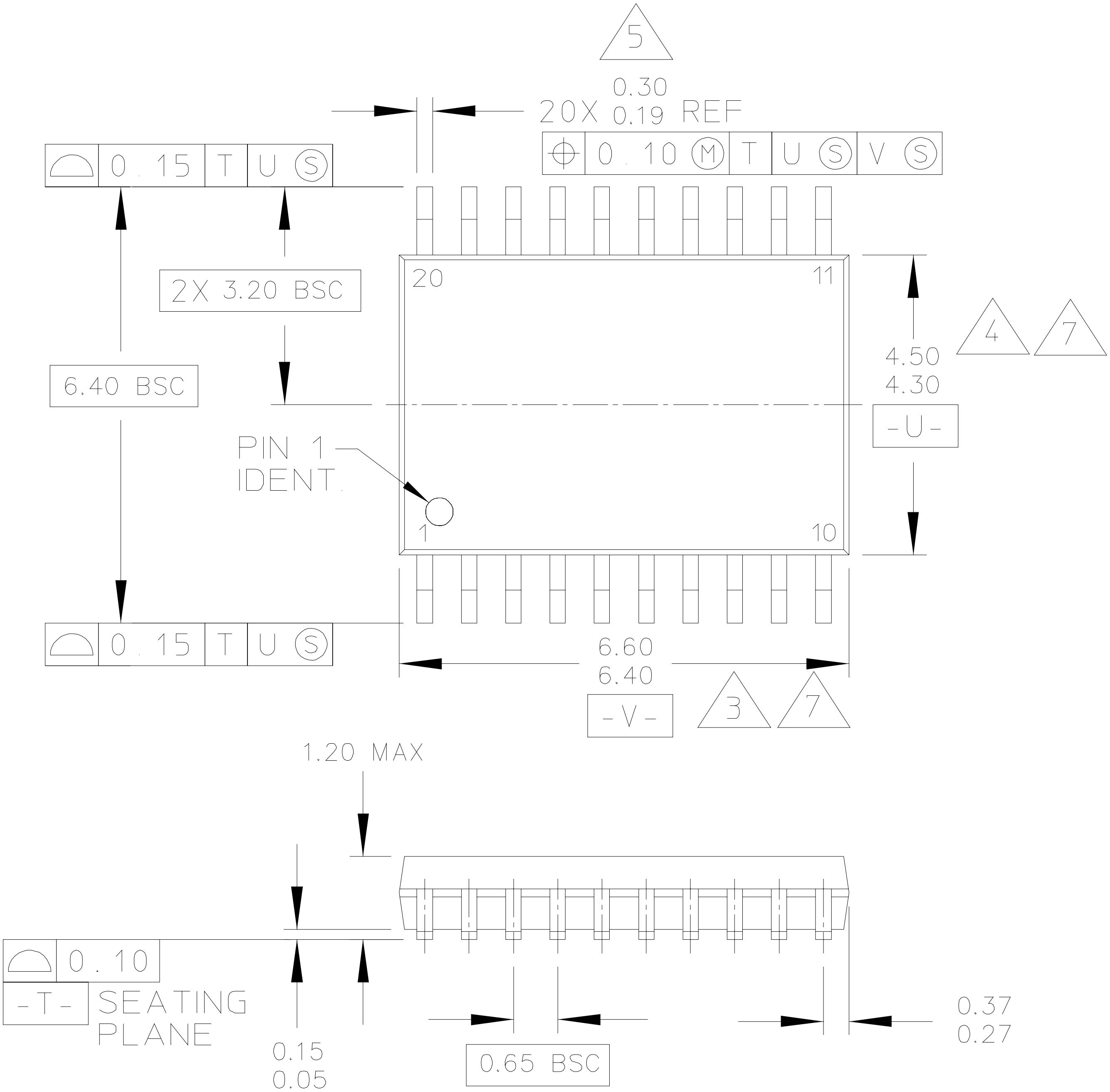
5 Package Information

Table 14. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
20	Thin Shrink Small Outline Package	TSSOP	TJ	948E	98ASH70169A
16	Thin Shrink Small Outline Package	TSSOP	TG	948F	98ASH70247A

5.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 14. For the latest available drawings, please visit our web site (http://www.freescale.com) and enter the package's document number into the keyword search box.



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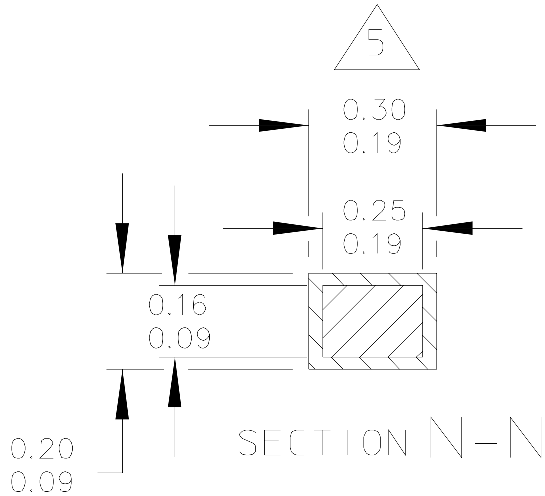
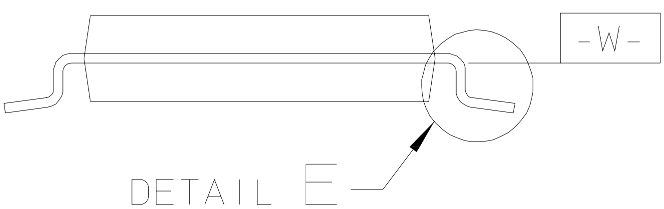
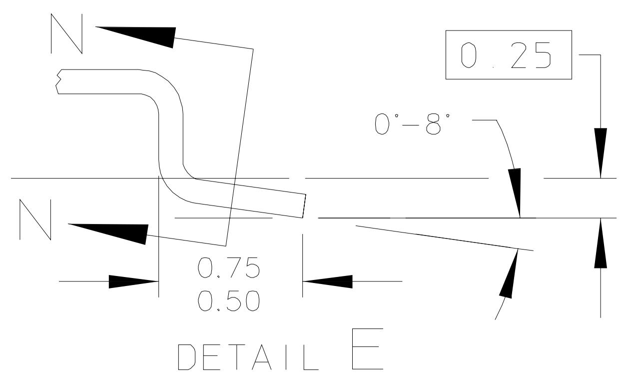
	CASE NUMBER: 948E-02	25 MAY 2005
	STANDARD: JEDEC	







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TITLE: 20 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70169A	REV: C
	CASE NUMBER: 948E-02	25 MAY 2005
	STANDARD: JEDEC	

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER

2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.

3. (△) DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

4. (△) DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5. (△) DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7. (△) DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

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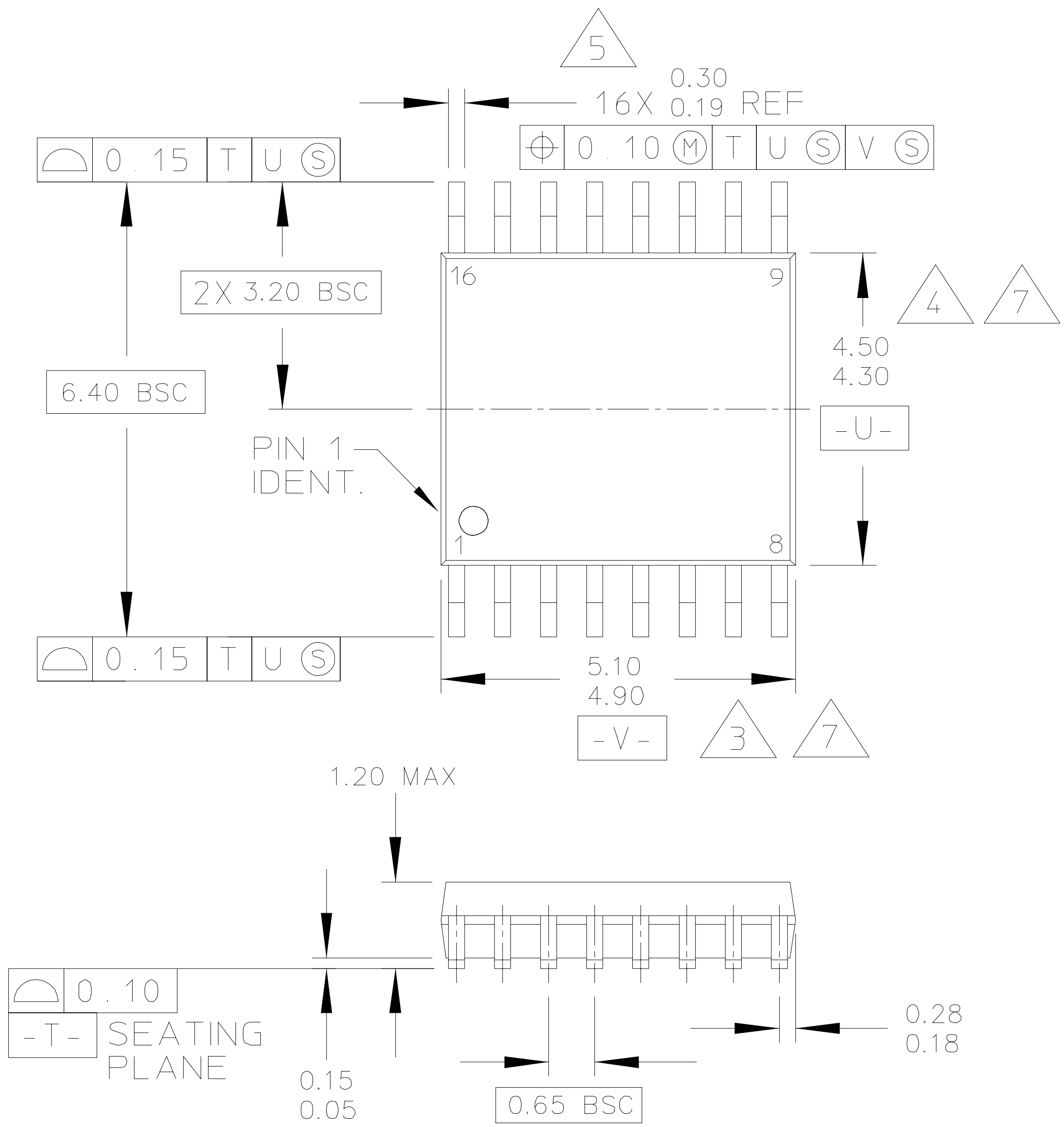
	CASE NUMBER: 948E-02	25 MAY 2005
	STANDARD: JEDEC	



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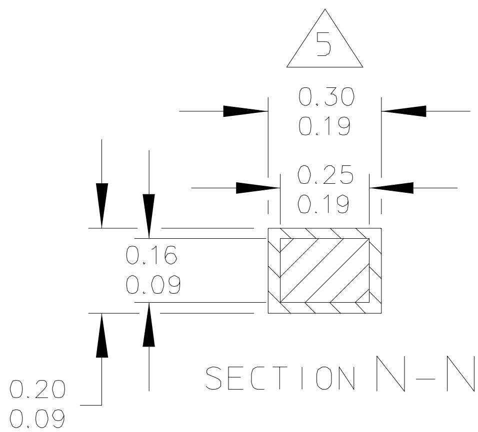

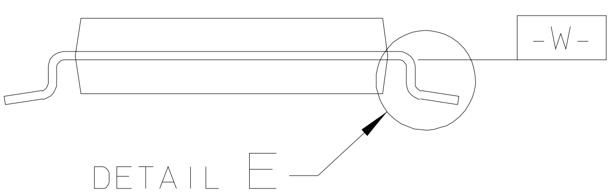

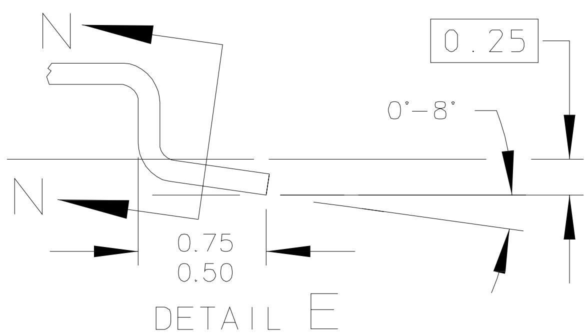

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 16 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70247A	REV: B
	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER

2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.

△3 DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

△4 DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

△5 DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

△7 DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

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	CASE NUMBER: 948F-01		19 MAY 2005
	STANDARD: JEDEC		

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